PATENT SPECIFICATION

(11) 1417721

(21) Application No. 53528/72 (22) Filed 20 Nov. 1972
(31) Convention Application No. 92433/71 (32) Filed 19 Nov. 1971
(31) Convention Application No. 97122/71 (32) Filed 3 Dec. 1971
(31) Convention Application No. 18083/72 (32) Filed 23 Feb. 1972
(31) Convention Application No. 30759/72 (32) Filed 29 March 1972
(31) Convention Application No. 75069/72 (32) Filed 28 July 1972
(31) Convention Application No. 83720/72 (32) Filed 23 Aug. 1972 in
(33) Japan (JA)
(44) Complete Specification published 17 Dec. 1975
(51) INT CL² H04N 1/38
(52) Index at acceptance

G1A 200 247 248 403 407 432 433 437 438 43Y 447 448 449 457 458 469 470 480 486 500 504 514 753

(19)

(54) IMPROVEMENTS IN OR RELATING TO DETECTION APPARATUS

(71) We, HITACHI LIMITED of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to apparatus for detecting small portions of a larger pattern. A particular application of the invention is for the detection and extraction of defects or bad spots from a pattern, and much of the following description deals with this, but it is to be understood that the invention is not so limited and references hereinafter to defects or bad spots should be read to include small pattern portions in general, where the context permits.

Previously, parts having complex patterns such as printed circuits or IC pellets have been examined visually by the inspectors, but since defective areas are generally included in the complex patterns of these devices and are very small in size, they may pass undetected very often, and a lengthy inspection is required, even by a skilled inspector. Furthermore eye fatigue is considerably increased when visual inspection is continued for a long time. In order to improve productivity and to save the labour cost, there has been devised and demonstrated an automated inspection equipment capable of detecting the defects included in a simple pattern in a plain background such as paper, glass, steel or the like, but so far no automated inspection equipment especially adapted for detecting bad spots or micro-defects included in a complex pattern such as a printed circuit or IC pellets has been proposed yet.

There has been proposed an inspection method in which a reference image which does not include any defect and consists of the areas or elements in two states such as bright and dark areas is optically registered with an image of a part to be inspected which includes bad spots or defects so that the latter may be indicated. The reference image must be registered with the image of a part to be inspected with a high degree of accuracy. For this purpose, a reference or standard object and a part to be inspected are securely held in position, and the reference object is illuminated with red light whereas the part to be inspected is illuminated with green light so that an inspector may see the images through a semi-transparent mirror. When the original perfectly coincides with the part to be inspected, the dark area becomes black whereas the bright area becomes white by combination of the red and green illumination. However a bright bad spot included in the dark area of the standard shows green whereas a dark bad spot included in the bright area of the standard shows red so that bad spots or defects may be easily seen. But this method has the disadvantage that the registration of the image of the reference object with the image of a part to be inspected must be made with an extremely high degree of accuracy so that this method may be carried out only by a skilled inspector. When there is a misalignment between the two images, the misaligned portions become green or red

so that they are mistakenly taken to be defects. Therefore this method is not entirely suitable for automated inspection equipment.

According to the present invention there is provided apparatus for detecting and extracting portions in a pattern including: input means for sequentially scanning a pattern to be inspected and converting said pattern into an electrical video signal; means for sampling said video signal at predetermined sampling time intervals corresponding to picture elements of said pattern to be inspected and converting said video signal into binary form; a two-dimension image extracting means for rearranging the one-dimensionally arranged output from said sampling and binary converting means into a two-dimensionally arranged signal representing a sub area of the pattern; and small portion processing means for extracting a signal from the information stored in said two-dimensional image extracting means, thereby extracting a small portion from said pattern.

The invention will be more particularly described by way of example with reference to the accompanying drawings, wherein:—

Figure 1 is a block diagram of an apparatus in accordance with the present invention;

Figures 2, 3 and 4 show the dark and bright patterns to be inspected by the apparatus of Figure 1;

Figure 5 is a block diagram of an apparatus incorporating a floating threshold type analogue-to-digital converter;

Figure 6 shows one example of the image of a pattern to be inspected;

Figure 7 is a block diagram of an apparatus similar to that shown in Figure 1 but including a two-dimensional image extracting device;

Figure 8 is a block diagram of an apparatus similar to that shown in Figure 7 but with a modification of the two-dimensional image extracting device;

Figure 9 is a block diagram of an apparatus similar to that shown in Figure 7 but with another modification of the two-dimensional image extracting device;

Figure 10 is a detailed view of a component of the apparatus shown in Figure 9;

Figure 11 is a view used for explanation of the apparatus shown in Figure 9;

Figures 12 to 15 are views used for explanation of the use of the boundary spacing method in the present invention;

Figure 16 is a detailed block diagram of the apparatus of Figure 1;

Figure 17 is a diagram of a micro-spot extracting circuit based upon the boundary spacing method;

Figure 18 shows the logic patterns used for the explanation of the boundary spacing method;

Figure 19 is a diagram of the boundary extracting circuit shown in Figure 16;

Figure 20 shows the logic patterns used for the boundary extraction method;

Figure 21 illustrates one example of a comparator used in the apparatus shown in Figure 16;

Figure 22 to 27 are views used for the explanation of the use of the enlargement-reduction method;

Figure 28 is a block diagram of an apparatus similar to that shown in Figure 1 except that a small portion processing device based upon the enlargement-reduction method is incorporated therein;

Figure 29 is a diagram of a small portion extracting circuit based upon the enlargement-reduction method;

Figure 30 is a perspective view of an optical processing device based upon the enlargement-reduction method to assist in the understanding of the invention;

Figures 31 to 35 are views used for the explanation of the use of the boundary averaging method in the present invention;

Figure 36 is a view used for the explanation of the bad spot extracting method;

Figure 37 is a block diagram of an apparatus similar to that shown in Figure 1 except that a micro-spot processing device employing the bad spot extracting method is incorporated therein;

Figure 38 shows the logic patterns used for the explanation of the bad spot extracting method; and

Figure 39 is a diagram of a micro-spot extracting device based upon the bad spot extracting method.

First there will be some explanation of some underlying principles of the present invention. The inspection equipment to be described is intended to inspect a multi-dimensional pattern consisting of two conditions, ON and OFF or light and dark, which are referred to as "binary states" in this specification. Therefore, the patterns may be a one-dimensional pattern such as telegraph codes, a two-dimensional

pattern which may be a visible pattern consisting of white and black areas, a three-dimensional pattern and so on.

For the following description of embodiment exemplifying the present invention, a two-dimensional pattern is used, but it will be understood that the invention is not limited thereto and can use any one- or multi-dimensional pattern.

A two-dimensional binary pattern is for example a black character or the like printed on a white paper, but it should be understood that it is not limited to such a pattern having a binary character in the strictest sense of the word. For example, the binary information may be derived from a multi-colour poster by using an optical filter, and even an object having a complex profile and surface pattern may be handled as a two-dimensional binary image when the object is illuminated against a suitable background.

In case of a two-dimensional multi-level pattern in which the tone is varied in steps or continuously in order to provide the contrast, the pattern may be converted into a two-dimensional pattern by a suitable threshold processing method.

Now, referring to Figure 1 illustrating a simple arrangement in accordance with the present invention, a component part 11 to be inspected is scanned by a video input device 12 such as a TV camera, and if necessary an optical filter (not shown) may be interposed between them. The video output signal from the video input device 12 is sampled by a sampling circuit 13 which may be of the type dividing the scanning signals of the TV camera by a predetermined time interval. The output signal of the sampling circuit 13 which varies in level depending upon the characteristics of the part 11 being inspected is converted into the binary signals representing the light and dark areas of the part 11 by a quantizing circuit (or AD converter) 14. (In this embodiment, the output signal of the video input device 12 is first sampled and then converted into binary signals, but it will be understood that the video output signal may be first converted into the binary signals and then sampled). The quantizing circuit 14 may be an analogue comparator or an AD converter whose multi-level output signals may be converted into the binary signals by suitable threshold level discriminating means. The present invention can use a fixed threshold method or a floating threshold method as will be described in detail hereinafter. The output of the quantizing circuit 14 is applied to a small portion processing device 16.

The small portion processing unit 16 may be an electronic computer, but instead of such an expensive computer specially designed hardware can be used adapted to accomplish (i) a boundary space process, (ii) an enlargement-reduction process, (iii) a periphery averaging process, and (iv) a small portion extracting process, all of which will be described in detail hereinafter, but it will be understood that the present invention is not limited to the above four methods. An alarm device or a colour television receiver is coupled as an output display device to an output terminal 17 of the processor 16.

In extracting the small portion of a multi-dimensional pattern, there may be used a simultaneous, parallel processing method or a sequential, serial processing method. The former has the advantage that the processing time is very fast but the disadvantage that the number of component parts is considerably increased, thus resulting in a high cost. The processing time by the sequential or serial processing method is not as fast as that of the simultaneous or parallel processing method, but can be of the order of 10 ms per picture or frame so that there need arise no serious problem in practice. The sequential processing is accomplished by a two-dimension buffer memory 15 shown in Figure 1.

The devices shown in Figure 1 will be described in more detail hereinafter.

Quantizing unit (AD Converter)

The continuous video signal from the TV camera is zero-clamped by a D.C. regenerating circuit (the black level being set to 0 V) and then converted into the binary signals by the fixed or the floating threshold method.

The fixed threshold method is the simpler. In it, the optical image of the part to be inspected is converted into continuous electrical signals by a scanning type photo-electric converter in the TV camera, and then converted into the binary signals by using a predetermined threshold level. The threshold level may be for example fixed to an intermediate level between the white and black levels of the image, but this has a disadvantage that only a bad spot or defect which is large in size may be detected whereas an extremely small bad spot cannot be sensed due to the limited resolution power of the photo-electric converter used.

Figure 2 shows the pattern of a part to be inspected which includes bad spots or defects. If the part to be inspected is an IC mask, the dark area represents for

example chrominum deposited upon a transparent glass plate. Bad spots in the dark area are indicated at 18 and 19, and in the bright area at 20 and 21. The video signal 23 is derived along the scanning line 22 passing through these bad spots, the voltage/time trace of the signal being shown below the part pattern. The spots appear in the video signal at 18′, 19′, 20′ and 21′ respectively. A threshold level 24 is fixed at a midpoint between the white and black levels. When the spots 19 and 21 are too small compared with the diameter of the electron beam, the levels of the signals 19′ and 21′ do not reach the threshold level 24. Therefore the binary signals 25 as shown in Figure 3 are produced and it is seen that the spot 19 and 21 in Figure 2 are not detected at all.

In the floating threshold method, the threshold level is varied depending upon the dark and bright levels of an image so that the bad spots 19 and 20 which are extremely small in size may be detected. For example as shown in Figure 2, a threshold level 26 is lowered when the level of the video signal level is low, but is raised when the latter is high. The centre or mean level of the floating threshold level 26 coincides with the fixed threshold level 24 and is slightly smaller than the level of the video signal 23. The signal representing a bad spot goes to the opposite direction of polarity to that of the signal representing the background provided the floating threshold level is varied sufficiently slowly with respect to the reversal in polarity of the video signal 23. Thus the binary signals 27 as shown in Figure 4 may be derived. It is seen that the video output signal is very fast to respond the reversal in brightness of the image at the bad spots and the boundary between the dark and bright areas. It is preferable that the level of the floating threshold 26 is as high as possible so far as it will not reach the noise levels in both the bright and dark levels. The floating threshold level is formed from the video signal. If the response time is too long, the signal representing a bad spot will not coincide with the actual spot, but if the response time is too short the resolution power is reduced. Therefore there must be a compromise between the response rate and the resolution power depending upon the image and hence a part to be inspected.

Figure 5 is a block diagram of an inspection equipment similar to that shown in Figure 1 and provided with the floating threshold type binary converter as described. The object 11 such as a printed circuit or an IC mask is scanned by the TV camera 12. A stationary threshold generator 28 gives a fixed threshold level depending upon the bright and dark levels of an image. A subtractor 29 subtracts the output signal of the generator 28 from the output signal of the TV camera 12 so that the centre level of the threshold level may be maintained almost at 0. The output 35 of the subtractor 29 enters a circuit 30 whose gain is slightly smaller than unity and which slowly trails the input signal. In practice the circuit 29 and 30 are operational amplifiers one of which is a linear delay line having a resistor and a capacitor inserted in the feedback loop and the other of which is an inverter with a gain less than unity for inverting the polarity. An adder 31 is adapted to add the output signal 36 from the circuit 30 to the output signal from the stationary threshold generator 28 so that the average level of the signal 36 may coincide with that of the video signal 33. The output signal 37 of the adder 31 is the floating threshold level 26 (Figure 2). A comparator 32 compares this signal with that from the TV camera 12 and gives "1" or "0" depending upon the difference therebetween. Thus, the output signal 38 of the comparator 32 corresponds to the signal 27 shown in Figure 4, that is the binary signal.

In the fixed threshold level generator 28 a constant voltage from a constant voltage source may be divided by a variable resistor, and the other circuits 29, 30, 31 and 32 may comprise simple operational amplifiers.

In this description the photo-electric converter 12 has been referred to as a TV camera for scanning the part 11 to be inspected so that the video signals are sequentially derived but the floating threshold level system may be also applied to a system in which a two-dimensional information is simultaneously processed by using a photo-electric converter 12 of the type capable of storing the focussed image such as an array of photo-electric cells and a memory of the type capable of storing an image which has uniform brightness over the whole area thereof and whose centre level, that is the spatial average, is fixed. The memory may be for example an array type frame memory. Instead of the subtractor 29, for example an array type operational amplifier group may be used for shifting the brightness of an image by subtracting the average brightness thereof. The circuit 30 is a filtering device such as a low-pass filter. The device 31 is an image adder and the device 32 is an image comparator. Therefore the output 37 of the image adder 31 becomes the two-dimensional

information in the form of a gentle waveform, and the steep image portion in excess of a given threshold level is extracted.

In case of the electro-cardiogram and electro-encephalography which handle very weak electrical signals, drift in the detectors can present a serious problem, but in the floating threshold system described the threshold level is varied in response to the slow drift so that the problem of drift is not serious when the signals are converted into the binary signals. Therefore even a very small peak which represents a bad spot may be easily detected.

Another advantage of the floating threshold system when applied to a pattern recognition device is that the shading of a TV camera or the like will not present a problem. That is, when the threshold level 24 is low in order to detect the bad spot 19′ in Figure 2, the black level is generally curved because of the non-uniform sensitivity of the camera tube. If a conventional fixed threshold system is used, the signal representing the normal black level other than a bad spot tends to exceed the threshold level, thereby mistakingly representing the white level. However when the floating threshold system is used, the erratic binary conversion due to non-uniform sensitivity such as shading may be prevented as far as the white and black levels of the video signal will not be overlapped, that is as far as they vary within the range outside of the centre level.

Two-Dimension Buffer Memory

This is a device for converting the two-dimensionally arranged information such as the optical, magnetic or mechanical information (which will be referred to below as "the pattern information") into the information of one dimension in time by scanning and then rearranging it into a two-dimensional pattern.

In a visual information processing system the image of an object obtained by a video input device such as a television camera is in general converted into signals representing the intensities of picture elements of the image. Conventional information processing of this type has been generally accomplished by a digital computer. A tremendous amount of video information is stored on a core or drum memory, and is processed in order to derive the characteristics of the object. For example when a picture frame is divided by 240 lines in the longitudinal direction and by 320 lines in the lateral direction, there are formed 76,800 picture elements. If six bits are used to represent the bright and dark picture elements, a large-capacity memory capable of storing 461 kilo bits is required. Furthermore each picture element must be processed. If it takes 100 micro seconds to process each picture element, it would take about 7.7 secs to process all of the picture elements. That the information stored in the memory is large and the processing time is long means that a large-capacity electronic computer must be used for a considerable time. Thus the cost of the inspection equipment becomes very high.

In contrast to such a system in which the video data are stored in a memory and then processed, the pattern information may here be immediately processed as soon as it is received. Thus there is the advantage that the pattern information may be processed at a speed equal to the input speed.

So far there has not been proposed an input device which is capable of simultaneously receiving all of the two-dimensional information. In general the video signals are derived for example by scanning by a television camera an object. In the two-dimension buffer memory shown here the two-dimensional space is converted by scanning into the one-dimensional time information which is converted into the two-dimensional information by use of a few memories so that the video information may be processed in a manner best adapted for attaining the required objects.

In video information processing it is often desired to remove the noise from an image of the type shown in Figure 6. For this purpose there has been proposed a very simple method for removing the noise from the signals obtained by scanning by using a time filter. However this is a one-dimensional system so that the components orthogonal to the scanning lines are not taken into consideration. In order to process the two-dimensional information, the information obtained by the previous scannings must be stored so that the orthogonal components may be also processed. In practice at least the information encircled by the area 39 in Figure 6 is preferably stored in the processing equipment. The simplest technical solution is to store all of the information of the image so that the required information encircled at 39 may be used at any time. This can be accomplished by a digital computer in the manner described hereinbefore, but a tremendous number of storage elements is required and a considerable time is required in writing and reading so that the processing equipment becomes complex in construction and expensive in cost. However

if only the information encircled by the area 39 in Figure 6 is stored and processed the number of storage elements may be reduced. Furthermore the information is processed as soon as the video information obtained by scanning is received so that the processing time may be considerably reduced. Thus the device may be constructed quite simply and may process the two-dimensional information at a high speed.

Thus, when the encircled information area 39 has m scanning lines each having a length l, the information corresponding to $m \times l$ is to be processed. If the $m \times l$ portion is capable of acting as a store, the storage capacity is such that only the information on $(m-1)$ scanning lines need be stored, not on m scanning lines. The equipment would be very complex in construction and expensive if the storage elements used for storing the information along the scanning line l is such that the continuously changing brightness information may be stored. Therefore a practical method is to divide the scanning line at a suitable interval depending upon the spacing between the adjacent scanning lines (in practice the scanning line l being sampled in time) and to quantize the sampled information for storage. If the scanning line l is divided into n segments and a number of k bits is used for quantization, the storage capacity for storing the information 39 will become $m \times n \times k$ bits. The quantized information may be stored by registers, delay lines or shift circuits using bubble memories.

Figure 7 shows one embodiment in which $m=3$, $n=4$ and $k=2$. The image input device such as a vidicon 12 is used in order to convert the optical image into the electric signals. A control signal generator 40 generates the sync signals and scanning signals to the image input unit 12 and to the sampling unit 13. In response to the scanning signal the video input unit 12 scans horizontally scanning in a manner well known in the art so that the two-dimensional dark and bright image may be converted into the one-dimensional electric information representing dark and bright information.

The electric information is sampled by the sampling circuit 13 in response to the control signal which is applied from the control signal generator 40 made in synchronism with the scanning signal. Therefore the scanning line l is divided into n segments. A quantization circuit such as AD converter 14 converts the analogue electric information into digital information in response to the sync signal applied from the control signal generator 40 in synchronism with the sampling period. Digital information derived from the quantization circuit consists of k bits.

Shift registers 41 and 41′ are adapted to store the quantized information on each scanning line and shift their contents toward the output in response to the sync signal applied from the control signal generator 40 in synchronism with the sampling frequency. Each shift register comprises $n \times k$ bit memory elements, and the output signal consisting of k bits is applied to the register 41 to the register 41′.

A shift register 42 consisting of $m \times n \times k$ bit memory elements stores the encircled information 39, and any bit may be written into and read out from the shift register 42. The output of the quantization unit 14 is applied to the input terminals (k terminals) of the lowermost stage of the shift register 42, the output of the shift register 41 to the input terminals of the middle stage, and the output of the shift register 41′ to the input terminals of the uppermost stage. All of the above outputs are applied in response to the sync signal from the control signal generator 40 in synchronism with the sampling frequency. Furthermore in response to the sync signal the k-bit signal in each stage is shifted to the right. The bit information stored in the shift register 42 is applied to the processing circuit 16 for processing the bit information. The output of the processing circuit 16 may be applied to another device or may be written into the shift register 42. The information processing by the circuit 16 is also effected in response to the sync signal applied from the control signal generator 40.

The image is scanned from left to right as in the case of the scanning used in the television so that when the right bottom corner of the encircled information area 39 is scanned, all of the information area 39 is stored in the shift register 42. The circuit 16 processing the information stored in the shift register 42 is coupled to other circuit the nature of which depend upon the objects of the data processing, but these are not within the scope of the present invention and no further description is necessary.

As the scanning and sampling operations proceed, the contents in the shift registers 41, 41′ and 42 are shifted. That is the information corresponding to one shift is stored in the shift register 42, and the output entirely different from the above information is derived from the processing circuit 16. As the image is scanned,

the processed information is derived from the processing circuit 16 so that when the output of the processing circuit 16 is arranged in response to the scanning signal from the control signal generator 40, the processed image may be obtained.

In another embodiment shown in Figure 8, instead of the shift registers 41 and 41′ shown in Figure 7, delay lines or analogue discs 43 and 43′ are used in order to store the analogue signals and instead of the sampling circuit 13 in Figure 7 sampling circuits 44, 44′ and 44″ which are actuated in response to the sync signals applied from the control signal generator 40 are provided. Furthermore instead of the quantization circuit 14 shown in Figure 7 three quantization circuits 45, 45′ and 45″ which are also actuated in response to the sync signals applied from the control signal generator 40 are provided. The mode of operation is substantially similar to that described with reference to Figure 7, so that no further description is required here.

Figure 9 shows a variation of the embodiment shown in Figure 7 for storing information for every j scanning lines into the shift register 42. The inputs to the shift registers 41 and 41′ are controlled by gates 46 and 46′ respectively, which in turn are controlled by the sync signals applied from the control signal generator 40 in synchronism with the scanning signals. In the present embodiment it may be assumed that $j=3$ and information on the first scanning line is stored in the shift register 42. In response to the scanning of the first line, the on signal is applied from the control signal generator 40 to the gates 46 and 46′ so that the gate for applying the output of the circuit 14 to the shift register 41 is opened whereas the gate for applying the output of the shift register 41 to the input terminal thereof is closed and similar the gate for applying the output of the shift register 41 to the input terminal of the shift register 41′ is opened whereas the gate for applying the output of the shift register 41′ to the input terminal thereof is closed. On the other hand, in response to the scanning of the second and third lines, an off signal is applied to the gates 46 and 46′ so that the gate for applying the output of the circuit 14 to the input terminal of the shift register 41 is closed whereas the gate for applying the output of the shift register 41 to the input terminal thereof is opened and similarly the gate for applying the output of the shift register 41 to the input terminal of the shift register 41′ is closed whereas the gate for applying the output of the shift register 41′ to the input terminal thereof is opened. In other words the contents in the shift registers 41 and 41′ are circulated when the second and third scannings are made. In response to the fourth scanning the operations described above with reference to the first scanning are cycled. In the manner described above the output signal of the circuit 14 is applied to the shift register 41 the content of which is transferred into the shift register 41′ for storage. Similarly the information for every third scanning line is stored in the shift register 42. In this manner the video information may be processed in a manner substantially similar to that described with reference to the first embodiment shown in Figure 7.

As shown in Figure 10, each of the gates 46 and 46′ may comprise an AND gate 47, a NAND gate 48 and an OR gate 49.

When it is desired to input coarse video information on a scanning line to the processing device 16, the output lines from the shift register 42 to the processing device 16 may be skipped as shown in Figure 11, and the width of the timing signal applied to the processing device 16 from the control signal generator must be increased accordingly. This arrangement is particularly advantageous when two different sets of information are processed in the processing device 16 and the information processing cannot be completed within the sampling period of the sampling circuit 13.

Small Portion Extracting Device

1. Boundary Space Method:

Figure 12 shows a part to be inspected in which the two-dimensional dark and bright pattern gradually changes its intensity at the boundary between the dark and bright areas. The bad spots or defects in the dark and bright areas are indicated by 50 and 51 respectively. Figure 13 shows an image of that shown in Figure 12 which is sampled and quantized at the binary level, and the bad spots which correspond to those 50 and 51 are indicated by 50′ and 51′ respectively. It is seen that the boundaries have a projection 52 and a recess 53 which are formed due to the quantization of the image. In the processing device the micro-spots such as 50′, 51′, 52 and 53 which may be the bad spots are extracted from the quantized image shown in Figure 13 and are detected whether they are bad spots or merely the

projection or recess at the boundary so that only the bad spots may be extracted or detected.

Next, referring to Figure 14 the principle of the method for extracting the micro spots which may be the bad spots or projections or recesses at the boundary will be described. The method for extracting a micro-spot off the boundary is to extract the picture elements whose brightness changes from bright, dark and bright or dark, bright and dark in one direction of the picture elements. For example the bad spots 50′ and 51′ may be detected because the brightness changes from bright, dark and bright and dark, bright and dark along the horizontal lines 54 and 55 respectively. However there is the possibility that a horizontally elongated micro-spot or bad spot may not be detected so that it should be monitored in the vertical direction and if required in an oblique direction. Therefore any bad spot may be detected with a required degree of accuracy in practice.

As for the extraction of the projections or recesses at the boundaries, two micro-regions are selected in such a manner that each picture element may be interposed therebetween. If one of the micro-regions is dark or bright when the other micro-region is bright or dark, then the projections or recesses at the boundaries may be identified. For example the projection 52 at the boundary is interposed between two micro-regions 56 and 56′, and the micro-region 56 is bright whereas the micro-region 56′ is dark so that the projection 52 may be identified. Similarly the recess 53 is interposed between two micro-regions 57 and 57′, and the former is dark whereas the latter is bright. When the micro-spots extracted in the manners described above are compared with each other, the bad spots 50″ and 51″ may be distinguished from the projection and recess at the boundaries as shown in Figure 15.

A processing device based upon this boundary space method will be explained with reference to Figure 16 which illustrates in block diagram of the equipment shown in Figure 1 and provided with the processing device. The optical image of a part 11 such as a printed circuit to be inspected is converted into electrical video signals by the photo-electric converter 12. A block 59 in the diagram indicates the binary conversion circuit 14, the sampling circuit 13, and a device 15 for extracting the two-dimensional micro-spot video information from the continuous video signal 58. The equipment further comprises a circuit 61 for extracting the micro-spots from the pattern based upon the above described boundary space method and a circuit for extracting the boundaries of the pattern. Instead of the device 61, a device based upon the enlargement-reduction or boundary averaging method to be described hereinafter may also be used.

The micro-spot or local video signal 60 is applied to both the micro-spot extracting circuit 61 and the boundary extracting circuit 62, and the output signals 63 and 64 of the circuits 61 and 62 are applied to the comparator 65 so that its output signal 66 may indicate only a true bad spot. This is displayed by a bad spot display device 67 such as a monitor TV. If required not only the bad spots but also the background may be displayed in different colours as shown in Figure 15 so that the position, sizes, types and the like of a bad spot may be more apparent.

One example of the small portion extracting circuit 61 is shown in Figure 17. Some examples of the portions of the image consisting of 5×5 picture elements are shown in Figure 18, and any micro-spot consisting of one or two picture elements is to be detected and extracted. In Figure 18, reference numeral 75 designates a logic pattern for detecting and extracting a micro-spot in the vertical direction, 76 and 77, those used in the horizontal direction, and 78, 79 and 80 and 81, those used in the diagonal directions.

The circuit 61 is shown in Figure 17 in conjunction with the logic patterns 74 and 75, and the output 70*a* becomes "1" when there is a micro-spot consisting of one or two picture elements in the vertical direction. 68*a*, 68*b*, 68*c* and 68*d* are AND circuits, and the inverted inputs are applied to the input terminals with the symbol *o*. 69 is an OR circuit. The circuit shown in Figure 17 is so arranged that its output 70*a* is "1" when the centre picture element 71 is "1" and both the picture elements 72 and 73 are "0" or when the centre picture element 71 is "0" and both the picture elements 72 and 73 are "1". Similarly from the logic circuits arranged for the logic patterns 76 to 81 shown in Figure 18 are derived the outputs 70*b*, 70*c* and 70*d* which are all "1". Consequently, when the picture element 71 is one of two adjacent picture elements or a single picture element, the OR circuit 63 gives the output "1".

One example of the circuit 62 for extracting the boundaries of the pattern is illustrated in Figure 19 and the logic patterns to be handled by the circuit 61 includ-

ing gates 201 to 208 shown in Figure 19 are illustrated in Figure 20. That is, the logic patterns 84 and 85 and those 86 and 87 are used to extract the boundaries having no defect in the diagonal, vertical and horizontal directions respectively. When the centre picture element 71 is taken into consideration and if the picture elements in the micro-regions 82 and 83 are all "0" and "1" or "1" and "0" respectively, the picture element 71 is identified as being located on the boundary having no defect. The picture elements including 71 but excluding the picture elements in the micro-regions 82 and 83 belong to the insensitive region. In Figure 19 the logic pattern 84 shown in Figure 20 is used so that when the boundary has no defect in the diagonal direction, the circuit 61 gives an output 88*a* of "1". Similarly in the logic patterns 85, 86 and 87 the outputs of the circuit 61 are "1" representing that the boundary has no defect. Thus, the output 64 becomes "1" when the centre picture element 71 is located on the boundary having no defect. Thus the boundary having no defect may be extracted by the spatial logic processing. It should be noted that the boundary portion extracting circuit 61 of the form described above may be used in combination with a small portion extracting device based upon the enlargement-reduction or boundary averaging method. In this case, a comparator 18 is inserted in the next stage.

Figure 21 shows one example of the comparator 65 for comparing the output 63 of the small portion extracting circuit 61 with the output 64 of the boundary portion extracting circuit 62. Only the true micro-spot or bad spot is indicated by this comparator 65. That is, when the centre picture element 71 is detected and extracted as a bad spot by the circuit of Figure 17 the output 63 becomes "1", but when the picture element 71 is detected by the circuit of Figure 19 as being located on the boundary, the output 64 becomes "1". Therefore the output 69 becomes "0" in this latter case so that the picture element 71 is identified as a projection or recess on the boundary. When the output 63 is "1" and the output 64 is "0", the output 69 becomes "1" which indicates that the picture element 71 is a bad spot off the boundary.

2. Enlargement-Reduction Method:

For the sake of explanation it is assumed that the part 11 to be inspected (Figure 1) has a pattern consisting of "1" and "0". For example the area "1" is taken into consideration. When the area "1" is two-dimensionally enlarged or expanded and then reduced again, the relatively small area "0" included in the area "1" disappears. Similarly when the area "0" is enlarged and then reduced two-dimensionally, the relatively small area "1" included in the area "0" disappears. The important feature of the enlargement and reduction method is that the area "1" or "0" is restored to its original configuration and position but the small area "0" or "1" included disappears.

Therefore it follows that when a two-dimensional pattern including a very minute defect is processed by the enlargement-reduction method, the same pattern not including the defect may be obtained. This restored pattern may be used for various purposes. The image of a printed circuit may be converted into the electrical signals, processed in the manner described above and then converted into an optical image again to remove defects.

The processed pattern may be compared with the original pattern so that only the defect area may be extracted as will be described in more detail hereinafter. Referring to Figure 22, the hatched area is assumed to be "1" and the white area "0". The area "1" includes a small area "0" indicated by 96 whereas the area "0" includes a small area "1" indicated by 97.

First the area "1" in pattern 89 of Figure 22 is enlarged; that is to say the boundary of the area "1" is enlarged or expanded toward the area "0" by the same distance so that the pattern shown at 90 in Figure 22 is obtained. By the above process, the area 96 is contracted and disappears whereas the area "1" is enlarged.

Next the area "1" in the pattern 90 is reduced, that is the boundary is reduced by the same distance toward the area "1" from the area "0" so that the pattern 91 is obtained. It is seen that the small area 96 is not restored, but the original area 89 is restored. In other words, the small area "0" included in the area "1" is eliminated as shown in the pattern 91.

By the comparison of the original pattern 89 with the processed pattern 91, a pattern 92 is obtained which includes the area "1" at the position corresponding to that of the defect or area "0" 89 of the original pattern.

When the area "1" of the pattern 89 is reduced, a pattern 93 is obtained. When the area "1" of the pattern 93 is enlarged or expanded, a pattern 94 is obtained. It

is seen that the relatively small area "1" at 97 included in the area "0" of the pattern 89 has disappeared. By the comparison of the original pattern 89 with the processed pattern 94, a pattern 95 is obtained which includes the area "1" at the position corresponding to that of the area "1" at 97 of the original pattern 89.

From the patterns 92 and 95, the small areas included in the original pattern 89 are all detected and extracted. It should be noted that the area "1" being reduced and enlarged means the area "0" being enlarged and reduced.

Next a practical illustration of the enlargement-reduction method will be described with reference to Figure 23 which shows two-dimensional patterns that are divided into a plurality of same square picture elements by the spatial sampling. Such a sampling method is widely used in the processing of images by digital equipment.

First each boundary of a picture element in the horizontal direction is displaced and then each boundary in the vertical direction is displaced. A pattern 98 to be processed has the hatched picture elements "1" and the white picture elements "0". The process for enlarging the areas "1" and then reducing them to their original size is illustrated at 99, 100, 101, and 102 and the process for reducing the areas or picture elements and then enlarging them to their original size is illustrated at 103, 104, 105, and 106. Only a micro-spot is processed to restore or eliminate it in the following description.

The elements "1" of the pattern 98 are enlarged in the horizontal direction so that the picture elements A and B in the pattern 99 change from "0" to "1". When the picture elements "1" including the horizontally enlarging picture elements are expanded in the vertical direction, the picture elements C and D in the pattern 99 are changed from "0" to "1" so that the pattern 100 is obtained. Next the picture elements "1" of the pattern 100 are reduced in the vertical direction so that the picture elements C′ and D′ of the pattern 101 are changed from "1" to "0", and when the picture elements are further reduced in the horizontal direction, the picture elements A′ and B′ are changed from "1" to "0" so that the pattern 102 is obtained. It is readily seen that the processed pattern 102 is the same with the original pattern 98 and that when a micro-area "1" is enlarged and then reduced, it is restored to its original configuration however small the micro-spot is. This means that the large and small areas "1" shown in the pattern 91 in Figure 22 are reproduced.

When the picture elements "1" in the pattern 98 are reduced in the vertical direction the picture elements C′ and D′ in the pattern 103 are changed from "1" to "0". When the picture elements "1" are further reduced or compressed in the horizontal direction, the picture element B′ is changed from "1" to "0" so that the pattern 104 is obtained. When the pattern 104 is enlarged or expanded, the pattern 105 and then the pattern 106 are obtained, but in practice since the pattern 104 does not include the element "1" there is no effective enlargement or expansion. Thus it is seen that when the picture element or elements "1" are reduced or compressed and then enlarged or expanded, the picture elements "1" disappear. This corresponds to the treatment of the area "1" at 97 which as is shown in the pattern 94 disappears by the reduction-enlargement method.

Next will be described a method for eliminating a micro-spot by the enlargement-reduction method without using the spatial sampling (that is, using a continuous pattern in space). It will be appreciated that the following description of a photographic method does not form any part of the invention claimed but is included herewith for a better understanding of the invention. This method uses photographic films (to be referred to as "film or films" hereinafter) and an unexposed film is overlaid upon an exposed and processed film and exposed by the light illuminated from the back of the processed film. It is assumed that the processed film has a pattern consisting of dark and bright areas so that when the film now exposed is developed or processed, the dark and bright areas are reversed. (This process will be referred to as "reversal processing" hereinafter in this specification). In some cases, a processed or original film and an unexposed film are expanded in all directions by the same extent while relative rotation between them is prevented. (This process will be referred to as "expansion reversal processing" hereinafter in this specification). An unexposed film is so processed that even a small area which has been exposed by the light transmitted through the light area of the original film even for a very short time may become a dark area. Similarly an area which has not exposed at all is processed to represent a bright area. The above-described conditions may be easily satisfied when high contrast films (which are readily available in the market) are used.

Next referring to Figures 24 and 25 the image forming process will be described in more detail hereinafter. An original image or pattern on a film has dark areas (shown hatched) and bright areas. The large dark area includes a bright micro-spot

118 whereas the large bright area, a dark micro-spot 117. First the method for eliminating these micro-spots will be described.

By the reversal processing a pattern 108 is obtained, and by the expansion reversal processing of the pattern 108, a pattern 109 is obtained. The pattern 109 includes the expanded or enlarged dark areas of the original pattern 107, and the micro-spot 118 in the dark area is eliminated.

By the expansion reversal processing of the pattern 109, a pattern 110 is obtained, and by the reversal processing of the pattern 110, a pattern 111 is obtained in which the dark area in the pattern 109 is compressed or reduced. The pattern or image 111 is substantially similar to the original pattern 107 except that the bright micro-spot included in the dark area in the original pattern 107 is eliminated.

From the foregoing description, a bright micro-spot included in the dark area of an original image or pattern may be eliminated by the process of enlarging the dark area and then reducing it (which is substantially similar to the process of enlarging the bright area and then reducing it).

From the comparison of the original image 107 with the processed film 111, the eliminated micro-spot may be readily detected. When the original film 107 is overlaid upon and registered with the processed film 110, only the bright micro-spot 118 may transmit the light so that it will be readily detected and extracted.

It is alternatively possible to extract the dark micro-spot 117 from the same original pattern 107 in the manner now to be described with reference to Figure 25. By the expansion reversal processing of the original image 107, a pattern 114 is obtained in which the dark micro-spot 117 is eliminated. By the reversal processing of the pattern 114, a pattern 115 may be obtained in which the dark area in the original image 107 is reduced or compressed.

By the reversal processing of the film 115, a pattern 114 is obtained, and by the expansion reversal processing of the pattern 114′, a pattern 116 is obtained in which the dark area in the pattern 115 is expanded or enlarged. Since the pattern 114 is substantially similar to the pattern 114′, by the expansion reversal processing of the original 107 the pattern 114 is obtained, and by the expansion reversal processing of the pattern 114, the pattern 116 is obtained, but in order to establish the one-to-one correspondence between the processes shown in Figure 24 and Figure 25, the patterns 114′ and 115 are illustrated and described.

In the pattern 116, the dark area in the pattern 115 is expanded or enlarged, and the pattern 116 is substantially similar to the original 107 except that the dark micro-spot 117 is eliminated.

From the foregoing description it is seen that the dark micro-spot included in the bright area may be eliminated by the process of reducing or compressing and then enlarging or expanding the dark area (which is equivalent to the process of enlarging or expanding and then reducing or compressing the bright area).

By the comparison of the original 107 with the pattern 116, the dark micro-spot 117 may be readily detected. When the patterns 108 and 116 are registered to each other, only the micro-spot 117 transmits the light so that it may be easily extracted. Alternatively when the patterns 110 and 116 are registered to each other, all of the micro-spots 117 and 118 included in the original pattern 107 may be readily detected and extracted.

Referring back to Figure 24, a pattern 112 is obtained by the expansion reversal processing of the pattern 111, and by the expansion reversal processing of the pattern 112, a pattern 113 is obtained in which all of the micro-spots 117 and 118 included in the original 107 are eliminated. It is seen that the pattern 113 is substantially similar to the original pattern 107 except for the eliminated micro-spots.

In the process for obtaining the pattern 113 from the original 107, the dark area is enlarged, reduced, and reduced and enlarged again (which is equivalent to the process in which the bright area is first reduced, enlarged and then enlarged and reduced again), and the micro-spots included in the original 107 are all eliminated. By the comparison of the original 107 with the pattern 113, the position and configuration of a micro-spot or bad spot may be easily detected. As described hereinbefore when the original 107 is registered with the pattern 110, the bright micro-spot 118 in the dark area may be detected and extracted, and when the pattern 108 is registered with the pattern 113, the dark spot 117 in the bright area may be detected and extracted.

In summary, when a dark or bright area in a two-dimensional binary pattern is enlarged in space by the same amount (distance) and then reduced by the same amount or first reduced by a predetermined amount in space and then enlarged by the same amount, any micro-spot included in the pattern may be eliminated. By the

comparison of an original pattern with the pattern processed by one or both of the above methods any micro-spot included in the original pattern may be extracted.

In general the defects or noise components included in a pattern are very minute so that they may be readily extracted by the processes described above.

The above processes do not require the registration required in general in the pattern recognition system. That is to say, there is no need to determine a correct relative position between a reference pattern which has been previously stored and an input image of a pattern to be recognized or inspected. Such registration can be extremely difficult because a pattern to be recognized or inspected might not completely coincide in detail with a reference pattern: this would follow from the fact that the part to be inspected would have various defects. Therefore the processes described are relatively simple in their application to the inspection of printed circuits, IC or printed characters. In a conventional system in which the registration is required, it is extremely difficult to detect and extract the defects or deformations unless a correct reference pattern is stored, but the processes described do not require the storage of a reference pattern so that the use of a storage device may be eliminated. Furthermore any new pattern which has been hitherto never processed may be equally as well handled.

In the processes described above, the amount of enlargement or reduction determines the size of a micro-spot or defect to be detected. Therefore the parameters used for the purpose of detecting a relatively large micro-spot or defect in a large pattern should not be used for detecting a relatively small micro-spot or defect in a small pattern. Such inspection conditions would generally be laid down in detail in the inspection specifications.

Next referring to Figure 26, a large number of storage elements are arrayed as shown at 119 and 120 in opposed relation with the space of an image. Any storage element may be used as far as information may be written into and read out from it, and in this embodiment flip-flops are used. In the arrays 119 and 120, each square defined by the broken lines represents a picture element in opposed relation with which is disposed each flip-flop or storage element.

Each flip-flop in the array 119 is turned on "1" or off "0" depending upon the corresponding picture element being bright or dark. For example when the image input device 12 is a television camera of the type scanning an object horizontally from the upper left to the lower right, the output signals from the quantizing circuit 14 are sequentially stored in the flip-flops in the array 119 from the upper left one to the lower right one. The above arrangement is well known in the art so that the further description will not be made.

The flip-flop array 120 which is substantially similar to the flip-flop array 119 serves to store the information to be processed in a manner now to be described. As shown in Figure 26, each flip-flop in the arrays 119 and 120 is identified by the coordinates (i, j).

An OR gate 121 serves for the enlargement process described hereinbefore. The contents in the five flip-flops $(i-1, j)$, $(i, j-1)$, (i, j), $(i, j+1)$ and $(i+1, j)$ in the array 119 are applied to the OR gate 121. The output of the flip-flop (i, j) in the array 120 is also applied to the OR gate 121. Similarly, such an OR gate is provided for every i and j. (For example when $i=1, 2, \ldots, m$ and $j=1, 2, \ldots, n$, the total of $m \times n$ OR gates are provided. The number of inputs to the OR gate is less than five when i and j approach l or m or n). Therefore the enlarged "1" is applied to the flip-flop array 120 from the flip-flop array 119.

For example when information is stored as shown in Figure 27 in the flip-flop array 119 (the hatched square represents the flip-flop state "1" whereas the white square, the flip-flop state "0"), information is stored in the flip-flop array 120 as shown at 123 in Figure 27. This means that the hatched areas are enlarged or expanded.

The method for storing in the flip-flop array 120 the reduced area information of the flip-flop array 119 may be accomplished by using AND gates instead of the OR gates 121 shown in, Figure 27. That is, the information stored in the flip-flop array 119 as shown at 123 in Figure 27 may be stored in the flip-flop array 120 as shown at 124 in Figure 27. This means that the hatched areas shown at 123 in Figure 27 are reduced as shown at 124.

The hatched areas shown at 122 are enlarged as shown at 123 and are reduced as shown at 124. It is seen that the small white area included in the main hatched area shown at 122 disappears in the pattern shown at 123, as is required.

The process is made in two steps in the manner described above so that the equipment may comprise in practice, firstly, means for storing the video information,

secondly, a plurality of OR gate means each of which is coupled to a plurality of predetermined storage elements in said video information storage means thereby giving the OR output of the outputs of said predetermined storage elements, thirdly, storage means for storing the outputs of said plurality of OR gate means, fourthly, a plurality of AND gate means each of which is coupled to a plurality of predetermined storage elements in said OR gate output storage means thereby giving the AND output of the outputs of said predetermined storage elements, and fifthly, storage means for storing the AND outputs of said plurality of AND gate means. The states of the third and fifth means are illustrated at 123 and 124 in Figure 27.

When the second and fourth means are exchanged, the hatched areas are compressed first and then enlarged. The state of the fifth means is illustrated at 126 in Figure 27 in which the small area "1" included in the large area "0" is eliminated. States of the first and third means are illustrated at 122 and 125 respectively.

In either of the arrangements in which the information or area is first compressed and enlarged or first enlarged and reduced, the number of $m \times n$ EXCLUSIVE OR gates may be provided in such a manner that the outputs of the corresponding storage elements in the first and fifth means may be applied to each of the EXCLUSIVE OR gates. Then the output "1" of the EXCLUSIVE OR gate means that the states of the corresponding storage elements in the first and fifth storage means are different. Therefore a small area included in a large area may be extracted, that is a bad spot or defect may be extracted.

Figure 28 shows in block diagram form an embodiment of the present invention based upon the above-described principle of the enlargement-reduction method. The binary output signals from the binary conversion circuit 14 are stored in a storage device 127 which is similar in construction and operation to the flip-flop array 119 shown in Figure 26. The information stored in the storage device 127 is processed by an OR gate network 128, which is similar in construction and operation to a plurality of OR gates 121 in Figure 26, to be applied to a storage device 129, which is similar in construction and operation to the flip-flop array 120 in Figure 26. The information stored in the storage device 129 is processed by an AND gate network similar in construction and operation to a plurality of AND gates described hereinbefore to be applied to a storage device 131 similar to the flip-flop array 120 in Figure 26. An EXCLUSIVE OR gate network 132 functions in the manner described above to give the exclusive OR output from the outputs of the corresponding storage elements in the storage devices 127 and 131. Networks 128′, 129′, 130′, 131′ and 132′ are similar in construction and operation to those 130, 129, 128, 131 and 132 respectively. An OR gate network 133 is provided to give the OR output from the outputs of the corresponding storage elements in the storage devices 132 and 132′. The output of the OR gate network 133 is stored in a storage device 134.

As described hereinbefore the storage elements which are "1" in the storage device 129 are the enlargement or expansion of the storage elements "1" in the storage device 127. The storage elements which are "1" in the storage device 131 are the reduction of the storage elements which are "1" in the storage device 129. The storage elements which are "1" in the storage device 129′ are the reduction of the storage elements which are "1" in the storage device 127. The storage elements which are "1" in the storage device 131′ are the enlargement of the storage elements which are "1" in the storage device 129′. Therefore the small "area" included in the large "area 1" in the storage device 127 is eliminated in the storage device 131. The small "area" "1" included in the large "area" "0" in the storage device 127 is eliminated in the storage device 131′. When the exclusive OR outputs are derived from the outputs of the corresponding storage elements in the storage devices 127 and 131, only the small area "0" included in the large area "1" in the storage device 127 is derived as "the area" "1". Similarly the small "area" "1" included in the large "area" "0" in the storage device 127 is derived as the "area" "1" when the exclusive OR outputs are derived from the contents in the storage devices 127 and 131′. When the OR outputs are derived from the outputs of the corresponding storage elements in the storage devices 132 and 132′, only the small "areas" in the storage device 127 are stored as "1s" in the storage device 134.

The networks 127—134 and 128′—132′ are illustrated in detail in Figure 29A. Only one vertical line is shown for the sake of simplicity, but the similar circuit components can be stacked perpendicular to the plane of the drawing in practice. The input terminals of the AND gates, OR gates and Exclusive OR gates which are arranged in a manner substantially similar to that described above are not shown also for the sake of simplicity.

Each square of the storage devices 127, 129, 131, 129′, 131′ and 134 represents

a storage element for each picture element and stores "1" or "0" depending upon whether the corresponding picture element is bright or dark. Reference numerals 128, 130′ and 133 designate the OR gate networks; 130 and 128′, the AND gate networks; and 132 and 132′, the EXCLUSIVE OR gate networks. Each EXCLUSIVE OR gate may be provided from two AND (NAND) gates 136 and 136′ and an OR gate 137 connected as shown in Figure 29B.

In the embodiment described here the centre picture element as well as four adjacent picture elements are processed, but it will be understood that the number of picture elements to be processed is not limited to five. When a bad spot or micro-spot to be processed is larger than a picture element, the number of picture elements to be processed must be increased accordingly. Furthermore in order to overcome the problem of directions of the enlargement and reduction, it is preferable to handle all of the picture elements included in a circle whose centre coincides with the centre picture element. When a pattern except a bad spot consists of a horizontally or vertically extending areas, it is preferable to handle or process a cross-shaped picture element as a centre element, that is a centre picture element extended in the vertical and horizontal directions.

In some cases it is more efficient to process the picture elements in step than to process all of the picture elements simultaneously. For example, instead of enlarging in both the vertical and horizontal directions by one picture element in the manner described with reference to Figure 26, the centre picture element may be enlarged only in the vertical or horizontal direction by one picture element. In this case, the similar result may be attained. The process described with reference to Figure 23 is this method. When the process is accomplished in step, the processing time is increased, but the processing equipment becomes simple in construction.

Next referring to Figure 30, an equipment for accomplishing the optical processing methods described hereinbefore with reference to Figures 24 and 25 will be described. It will again be appreciated that the following description with reference to Fig. 30 and Figs. 24 and 25 does not form any part of the invention claimed and is only included to assist in the understanding thereof. In practice a condenser lens (not shown) is interposed between a light source 138 and an original film 139 in order to provide the uniform illumination. An unexposed film 140 is placed upon a frame 143. The original film 139 corresponds to the original pattern 107 in Figures 24 and 25 whereas the unexposed film 140 is used to obtain the pattern 108. When the pattern 108 shown in Figures 24 and 25 is used as the original film 139, the unexposed film 140 is used to obtain the pattern 108. The image on the original film 139 is focussed at the same size through a projection lens 141 upon the unexposed film 140 placed on the frame 143. The original film 139 is placed upon a frame 142 which in turn is slidably placed on a frame 144 which in turn is placed upon a frame 145 for slidable movement in the longitudinal direction. The positions of the light source 138, the frame 145 and the lens 141 are fixed.

An operating lever 146 whose one end is fixed to the frame 142 has an aperture 147 through which extends a pin (not shown) extending from the frame 145 so that the movement of the frame 142 by the operating lever 146 is limited by the engagement of the pin with the aperture 147. Furthermore the rotation of the frame 142 is prevented.

Next the mode of operation will be described. First the light source 138 must be turned off and the operating lever 146 is adjusted so that the pin is located at the centre of the aperture. The holder 143 is adjusted so that the image of the original film 139 may be focussed through the projection lens 141 upon the unexposed film 140. Next the lamp 138 is turned on and the operating lever 146 is actuated in such a manner that the pin is run around the edge of the aperture 147. Thereafter the lamp 138 is turned off and the exposed film 140 is processed. Thus the expanded and reversed image is obtained. When it is desired to obtain a reversal image, the operating lever 146 must be maintained stationary.

The above exposure process must be made in the dark room. It is preferable to use a high contrast film such as a film used for preparing a printing plate. The aperture 147 in the operating lever 146 must be determined depending upon the enlargement or reduction amount or scale and of course upon the size of the pin. In general the aperture is circular in order to eliminate the problem of the direction of the enlargement or reduction, but in some cases an aperture may have a special configuration depending upon the purpose. The position of the holder 143 must be correctly determined because it in turn determines the distance between the original film 139 and the unexposed film 140 and also the accuracy in registration between two processed films when they are registered with each other in order to extract a micro-spot

in the manner described with reference to Figure 24 with the two patterns 110 and 107. It is therefore preferable that the holder 143 is located in a predetermined position in the equipment.

The equipment of the type described above may be used for example for correcting a pattern having a micro-spot or bad spot. A pattern which is used for manufacture of printed circuits or the like and which has bad spots or defects caused in drawing the pattern may be corrected by this equipment. Furthermore an original film used for printing a number of copies may be also corrected by this equipment so that the original film may have no defect or flaw. The equipment can also be used to provide a pattern only showing the bad spots.

When the printed circuits which are manufactured with a pattern having a sharp angle are inspected by the equipment of the present invention, a portion having a sharp angle may be detected as a defect or bad spot. However when the original pattern used in the inspection is corrected in the manner described above, the portion having a sharp angle may be eliminated so that this portion may be prevented from being mistakingly extracted as a bad spot. Therefore the equipment may be used for preparing a reference pattern best adapted for use with the micro-spot inspection equipment in accordance with the present invention. It is of course understood that a reference pattern in which a sharp angle portion included in an original pattern will not adversely affect the result of the inspection of the parts manufactured from the original pattern.

As described hereinbefore an area in one binary state in a two-dimensional binary pattern is enlarged or reduced in the two-dimensional space and then reduced or enlarged so that the micro-spots or bad spots included in the pattern may be eliminated.

By comparing the original pattern with a pattern obtained by one or both of the methods described above, only the micro-spots or bad spots included in the original pattern may be detected and extracted. In enlargement and reduction the boundary line is preferably enlarged or expanded and reduced or compressed in the direction perpendicular to the boundary line, but the present invention is not limited to this method alone.

The eliminated or extracted micro-spot or bad spot is very closely related with the expansion and compression of the boundary line. The higher the degree of expansion or reduction, the larger the size of the eliminated or extracted micro-spot or bad spot becomes.

Therefore when it is desired to eliminate or extract a micro-spot or bad spot according to the present invention, it is preferable that the pattern (which must be the correct pattern having no defect or flaw) is larger in size than a bad spot. When the sizes of the original pattern and the defect are different, only the defect may be eliminated or extracted without adversely affecting the original pattern by suitably selecting the displacement of the boundary line in expansion or reduction.

Even if the above conditions are not fully satisfied, a bad spot or defect may be partly eliminated or extracted and when the same process is cycled, the bad spot or defect may be completely eliminated or extracted. Therefore there is no problem in practice. For example a bad spot included in a printed circuit is generally smaller in size than the conductor and non-conductor patterns. When a relatively large defect intersects the original pattern such as a conductor pattern, the intersection generally has an acute angle so that a gap between the defect and the original pattern tends to be detected as a micro-spot or bad spot. Therefore a relatively large defect may be detected from the gap between the defect and the original pattern which is detected in the manner described above.

A relatively small spot included in an original pattern may be eliminated or extracted so that a complex pattern may be corrected, that is a pattern from which the noise components are entirely removed may be provided. Alternatively only the defects or noise included in a complex pattern may be reproduced as a pattern.

For example a thin portion and an un-printed portion of a character pattern may be corrected so that a correct character pattern may be provided for display or the like. When the present invention is applied to the pattern or character recognition system, the character recognition efficiency may be much enhanced. Furthermore only the defects may be extracted and displayed as a measure of correction.

3. Boundary Averaging Method:

The boundary averaging method for extracting or eliminating a micro-spot included in a pattern will initially be described with reference to Figure 31. First a central point 149 in a pattern 148 is selected and the area surrounding the central

point 149 is investigated. If the surrounding areas "1" or "0" are larger in number than the areas "0" or "1", then the central point 149 is determined to have "1" or "0" and a new pattern 149′ which represents "1" or "0" is generated at the position corresponding to the central point 149. The above operation is cycled over the whole surface of the pattern 148 so that a micro-spot included in the pattern may be eliminated. In Figure 31, a two-dimensional sampled pattern or image is illustrated, but the boundary averaging method may be also applied to a continuous or sampled pattern or image. In case of the continuous image, the area "1" is compared with the area "0". In the method illustrated in Figure 31, 13 picture elements surrounding the central picture element 149 are investigated, but the number of picture elements to be investigated may be determined depending upon the size of a micro-spot to be detected. In case of the continuous image the threshold level is determined to be one half of the area to be investigated.

A device 150 is so arranged that when the number of inputs "1" or "0" from the surrounding picture elements is in excess of one half of the surrounding picture elements investigated, the device 150 outputs the signal "1" or "0".

Next the boundary averaging method will be described with reference to a simple one-dimensional image or pattern. Figure 32A shows a device for generating a pattern by the parallel processing of a one-dimensional image which is sampled, and Figure 32B a device for generating a pattern by the sequential processing of a one-dimensional image which is sampled. Devices 150*i*, 150*j*, 150*k* . . . and 150*p* are illustrated in detail in Figure 33. A device 150′ shown in Figure 32B can also be similar to that shown in Figure 33. It is assumed that a picture element 152 is selected to generate a pattern 152′. In this case two adjacent picture elements 151 and 153 are investigated together with the picture element 152, and the outputs are applied to the input terminals 160, 161 and 162 of the device 150*i*. If more than two outputs are applied to the device 150*i*, a voltage across a resistor R_1 is obtained such that a gate 164 is opened and an output is produced at an output terminal 163. As a result the pattern "1" or "0" is generated at 152′. In the similar manner described above, the patterns 153′, 154′, . . . are generated.

In the device shown in Figure 32B both the original and generated patterns are simultaneously shifted in order to generate the patterns only by one device 150′.

The parallel and sequential or serial processing devices described above with reference to Figure 32 may be also applied to a n-dimensional image or pattern which is sampled, but description of this is not necessary as the arrangement will be apparent to those skilled in the art from the above explanation.

Figure 34 shows a variation of the device for generating a pattern by the parallel processing of a one-dimensional image which is sampled. (A) and (F) show an original pattern, (B) and (G), the original pattern shifted to left, (C) and (H), the original pattern shifted to right, (D) and (I), a pattern formed by the addition of the original pattern and said patterns shifted to right and left, (E) and (J), a binary-coded pattern of the addition pattern, and (K), a pattern generated as a function of the combined patterns shown at (F), (G), and (H). It is seen that the sum of any three adjacent picture elements in A is same as the picture element in (D) which corresponds in position to the central picture element of the three adjacent picture elements in (A).

Figure 35 shows a diagram of a circuit for processing serially a one-dimensional continuous image. Reference numerals 165 and 166 denote an input and output terminal respectively, and D_1—D_n, delay lines. The output of an original pattern is applied to the input terminal 165 and thus to the delay lines D_1—D_n. When the voltage across a resistor R_2 becomes higher than a predetermined level, a gate 167 is opened and an output is derived from the output terminal 166 for generating a pattern.

4. Small Portion Extracting Method

Opposed to the boundary spacing method, the enlargement-reduction method and the boundary averaging method described hereinbefore, the small portion or bad spot extracting method does not require a boundary extracting circuit. Any of the micro-spot extracting circuits based upon the above three methods may be used as a micro-spot processing equipment, but they tend to detect the projections and notches on the boundary lines as defects. Therefore these circuits must be used in combination with a boundary extracting circuit of the type described hereinbefore.

However the processing equipment based upon the bad spot extracting method to be described in detail hereinafter may attain both the functions of the micro-spot extracting circuit and the boundary extracting circuit.

Referring back to Figure 13, the hatched areas represent a copper foil on a printed circuit or chrominum or emulsion on an IC mask. The bad spots 50 and

50′ are included in the dark and bright areas. The projection 52 and the notch 53 are formed at the boundary lines due to the sampling of the pattern.

The equipment based upon the micro-spot extracting method has an advantage that only the bad spots 50′ and 51′ are extracted but the projection 52 and the notch 53 on the boundary lines are not detected and extracted.

Next referring to Figure 36, a picture element 168 is selected and regions 169*a* to 169*n* that surround the picture element 168 are investigated. The configuration and size of the surrounding regions 169*a* to 169*n* are selected depending upon the complexity of an original pattern to be inspected. Preferably the surrounding region is in the form of a segment, an egg, an ellipse or the like whose elongated portion is directed toward the selected picture element 168 and has a length less than one half of the width of a normal pattern.

Next the method for determining whether the picture element 168 is a defect or a normal pattern will be described. It is assumed that the picture element 168 is in a logic state Po ("1" or "0"). The picture element 168 is detected as a part of a normal pattern when and only when all of the picture elements included in at least one surrounding region 169 are Po. In other words, when the logic function

$$F_0=\left\{P_0\cap\left(\bigcup_{j=1}^{m}\bigcap_{i=1}^{n}P_i^j\right)\right\}\cup\left\{\bar{P}_0\cap\left(\bigcup_{j=1}^{m}\bigcap_{i=1}^{n}\bar{P}_i^j\right)\right\}\qquad(1)$$

where P_1^j—Pn^j designate the logic states of the picture elements 170*a*—170*n* included in the surrounding region 169*j*,

gives "1", the picture element 168 is identified as a part of a normal pattern. Therefore the logic function

$$G_0=\bar{F}_0=\left\{P_0\cup\left(\bigcap_{j=1}^{m}\bigcup_{i=1}^{n}P_j^i\right)\right\}\cap\left\{\bar{P}_0\cup\left(\bigcap_{j=1}^{m}\bigcup_{i=1}^{n}\bar{P}_i^j\right)\right\}\qquad(2)$$

gives "1" when the picture element 168 is a bad spot or defect. The logic function G*o* always gives "1" when at least one of the picture elements included in the surrounding region is not Po. Therefore the logic function G*o* gives "1" when the bad spots 50 and 51 (Figure 13) are detected, but gives "0" for the projection 52 and the notch 53 on the boundary lines. Therefore from the binary pattern shown in Figure 13 is including the bad spots the pattern shown in Figure 15 may be directly obtained. In Figure 15 the micro-spots 50″ and 51″ correspond to the bad spots 50′ and 51′ in the pattern shown in Figure 13. If the extracted bad spots and the background are displayed in different colour on a colour display device, the sizes, types, positions and the like of the bad spots may be easily detected.

Next an equipment using this micro-spot extracting method will be described with reference to a block diagram shown in Figure 37. The optical image of a part 11 to be inspected such as a printed circuit or IC mask is converted into an electrical signal by a photo-electric converter 12 such as a television camera. The video signal 171 from the camera 12 is converted into the binary coded signals 172 by an analogue-to-digital converter 14. A device 15 extracts sequentially the two-dimensional local video signal 173 from the binary coded and sampled video signal 172. A small portion processing device 174 is adapted to extract a bad spot from the local video signal 173, and an extracted bad spot signal 175 is displayed by a bad spot display unit 176. The display unit 176 may be a colour display device for displaying a bad spot in colour and if required the background from the signal 172 as shown in Figure 35.

Figure 38 shows some examples of the binary coded and sampled patterns which are to be processed according to the principle of the micro-spot extracting method described above. 178 is a central picture element, and 179 to 186 are the picture element regions which are subjected to the space logic processing in accordance with the present invention. Since the image is sampled, the regions are different in configuration depending upon the directions. The surrounding regions 179 to 186 must be so selected as to completely encircle the central picture element 178.

Figure 39 shows a circuit for accomplishing the above logic function (1). An AND gate 187 gives the output 188*a* of "1" when all of four picture elements included in the region 179 of the two-dimensional local video signal 173. Similarly when and only when all of the picture elements included in the surrounding regions

179 to 186 are "1", the outputs "1" 188*b*—188*h* are derived. If all of the picture elements in any of the regions 179 to 186 are "1", the output of an OR gate 189 becomes "1", and if the central picture element 178 is "1", the output of an AND gate 191 becomes also "1". Then the central picture element 178 is detected as a part of a normal pattern so that the output 175 of a NOR gate 183 becomes "0". Similarly, when the central picture element 178 is "0" and if all of the picture elements in any of the surrounding regions 179 to 186 are "0", the output of an AND gate 193 becomes "1" so that the output 175 of the NOR gate 192 becomes "0". When each of the surrounding regions 179 to 186 includes a picture element opposite to the central picture element 178, the latter is detected as a part of a bad spot or defect and the NOR gate 192 gives the output "1".

As described hereinbefore according to the present invention the local video signals of a dark and bright pattern image are sequentially derived and a true bad spot included in the local video signal is detected and extracted. Therefore the projections or notches on the boundary lines may be prevented from being mistakingly detected and extracted as a defect, and the bad spots on the printed circuits or IC pellets having the complex patterns may be easily detected and extracted. Furthermore only the bad spots or defects may be displayed on a display device, and an alarm device may be actuated when the number of bad spots reaches a predetermined number. Moreover in response to the signal of the alarm device, a device for continuously or intermittently feeding parts to be inspected into the micro-spot or bad spot inspection equipment may be temporarily stopped, and a part such as a printed circuit having a bad spot may be rejected automatically.

WHAT WE CLAIM IS:—

1. Apparatus for detecting and extracting portions in a pattern including: input means for sequentially scanning a pattern to be inspected and converting said pattern into an electrical video signal; means for sampling said video signal at predetermined sampling time intervals corresponding to picture elements of said pattern to be inspected and converting said video signal into binary form; a two-dimension image extracting means for rearranging the one-dimensionally arranged output from said sampling and binary converting means into a two-dimensionally arranged signal representing a sub area of the pattern; and processing means for extracting a signal from the information stored in said two-dimensional image extracting means, to thereby extract a small portion from said pattern.

2. Apparatus according to claim 1, wherein said two-dimensional image extracting means comprises: first memory means, in which one element or a plurality of elements connected in series, each store the pattern information per one scanning line obtained by said sequential scanning and for shifting said stored pattern information in response to the shift of the scanning point of said pattern information which is made in response to a sync signal in synchronism with a scanning signal, and second memory means for storing the input information applied to the first element in said first memory means and the outputs of all said elements in said first memory means and for shifting said stored information in response to said sync signal.

3. Apparatus according to claim 1 or 2, wherein said means for converting said video signal into a binary coded video signal comprises: means for subtracting from said video signal a predetermined signal level; means for reducing the amplitude of the output from said subtracting means and for smoothing the reduced output; means for adding said predetermined signal level to the output of said reducing and smoothing means; and means for converting said video signal into a binary coded video signal with the output of said adder means as a threshold.

4. Apparatus according to claim 3, wherein said small portion processing means comprises: a small portion extracting circuit for providing an output when the number of the binary coded signals representing one of the two states of a plurality of picture elements included in any of a plurality of continuous patterns passing through a predetermined picture element in a plurality of directions is less than a predetermined number; a boundary portion extracting circuit for providing an output when the binary signals representing the binary states of two local areas which are selected in a plurality of directions with an insensitive region, including said predetermined picture element being interposed between said two local areas, are different from each other; and a comparator for receiving the outputs of said small portion extracting circuit and said boundary portions extracting circuit and for generating an output when and only when said boundary extracting circuit does not generate an output.

5. Apparatus according to claim 3, wherein said small portion processing means

includes first processing means comprising: means for compressing and then expanding the binary coded video signal in one state; and means connected to said compressing and expanding means for expanding and then compressing said binary coded video signal in one state.

6. Apparatus according to claim 5, wherein said small portion processing means further includes: second processing means for comparing an original pattern with a pattern which is obtained by said first processing means, and in which a small portion is eliminated and extracting said small portion included in said original pattern.

7. Apparatus for detecting and extracting small portions in a pattern constructed and arranged for use and operation substantially as described herein, with reference to and as illustrated in Fig. 1, or Fig. 5, or Fig. 7, or Fig. 8, or Fig. 9, or Fig. 16, or Fig. 28 or Fig. 37 of the accompanying drawings.

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Agents for the Applicants.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1975.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

FIG. 1

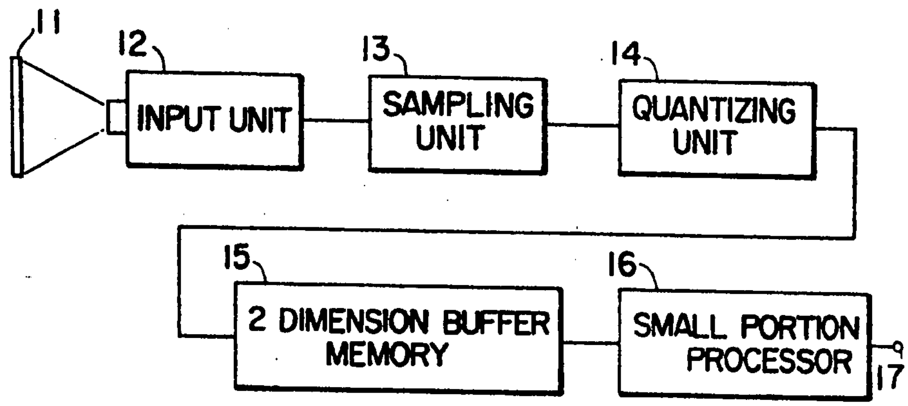


FIG. 2

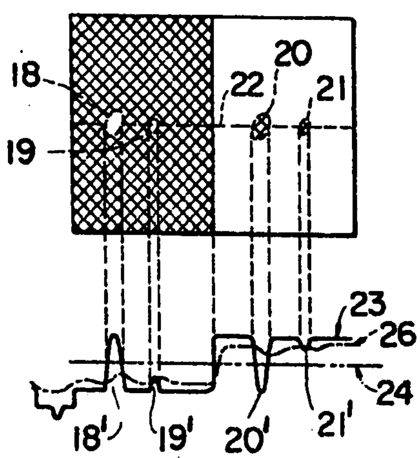


FIG. 3

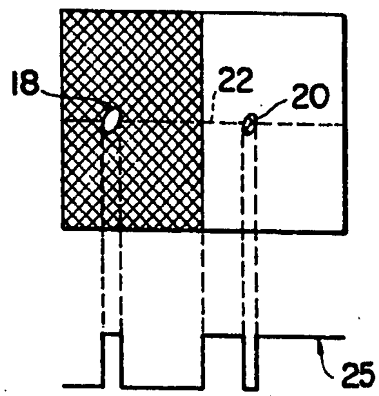


FIG. 4

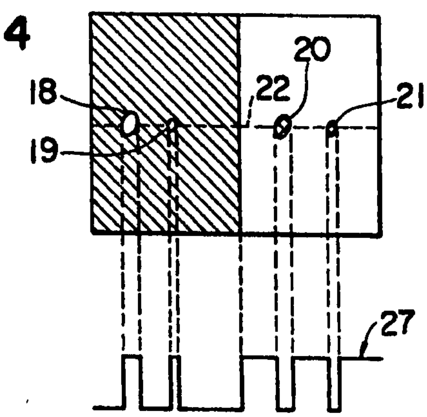


FIG. 5

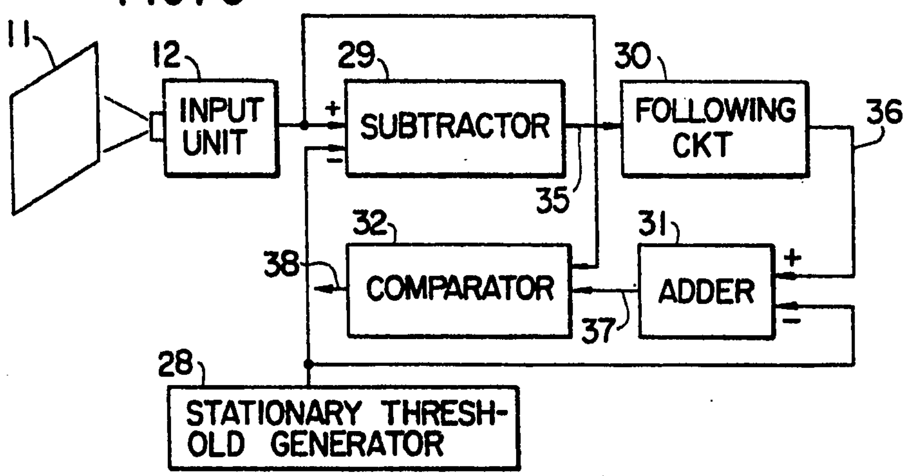


FIG. 6

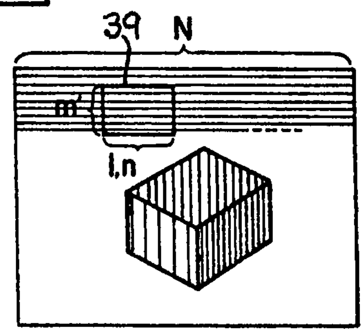


FIG. 7

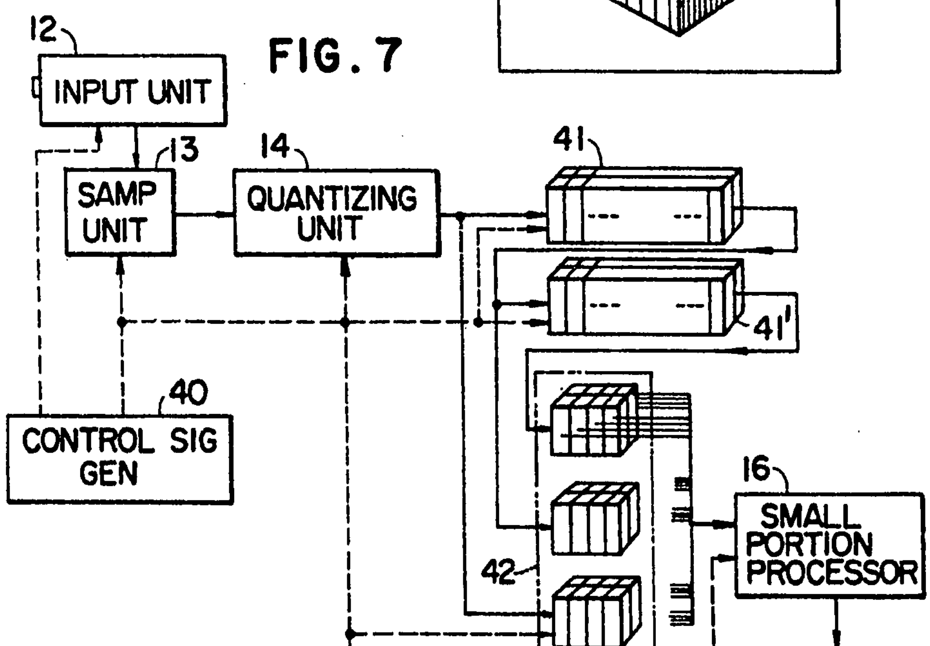


FIG. 8

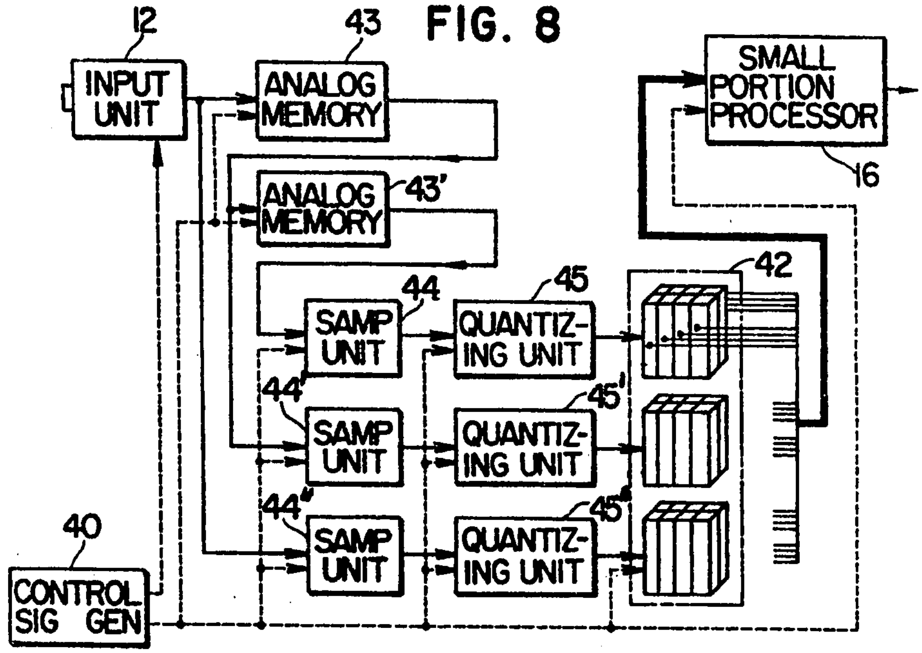

12
INPUT UNIT
43
ANALOG MEMORY
ANALOG MEMORY
43'
SMALL PORTION PROCESSOR
16
42
44
45
SAMP UNIT
QUANTIZ-ING UNIT
44'
45'
SAMP UNIT
QUANTIZ-ING UNIT
44"
45"
SAMP UNIT
QUANTIZ-ING UNIT
40
CONTROL SIG GEN

FIG. 9

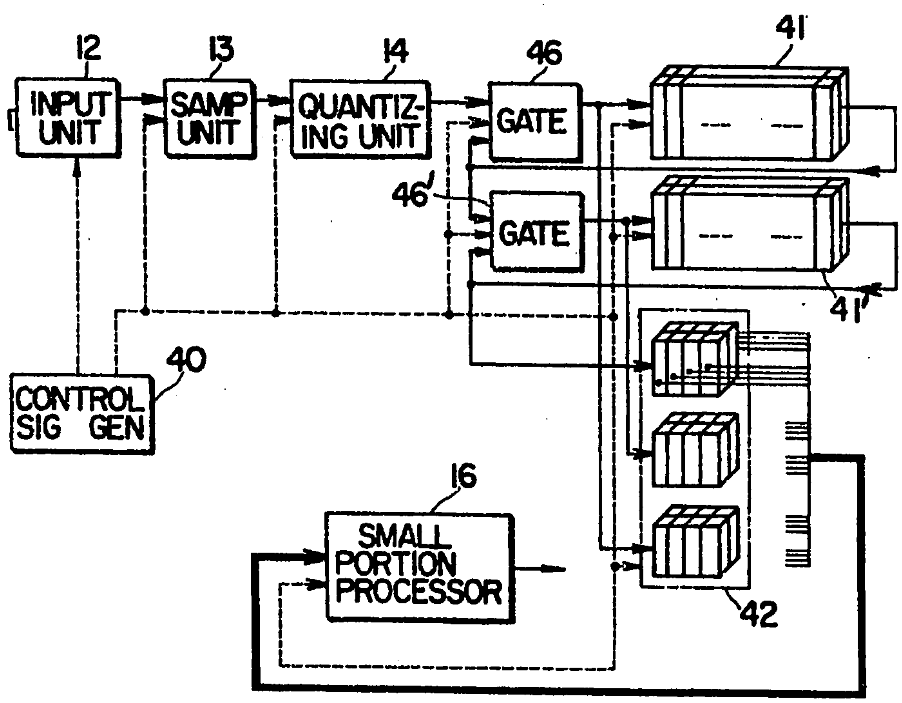

12
13
14
46
41
INPUT UNIT
SAMP UNIT
QUANTIZ-ING UNIT
GATE
46'
GATE
41'
40
CONTROL SIG GEN
16
SMALL PORTION PROCESSOR
42

FIG. 10

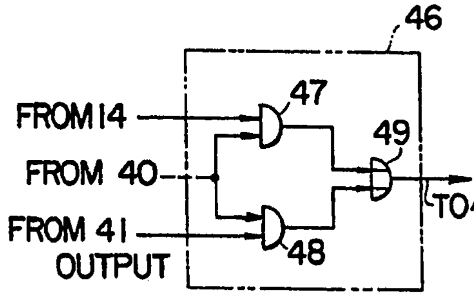


FIG. 11

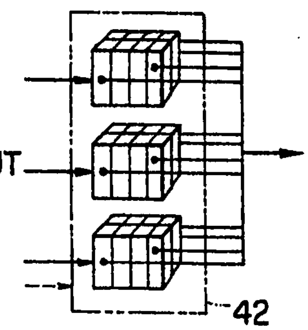


FIG. 12

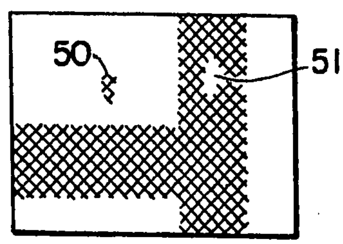


FIG. 13

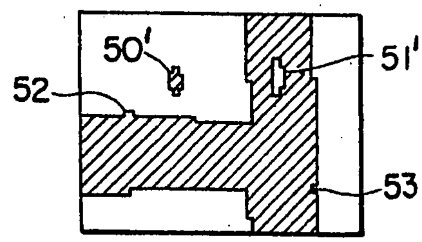


FIG. 14

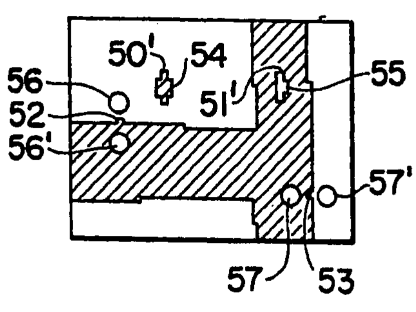


FIG. 15

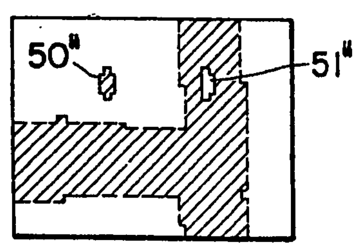


FIG. 16

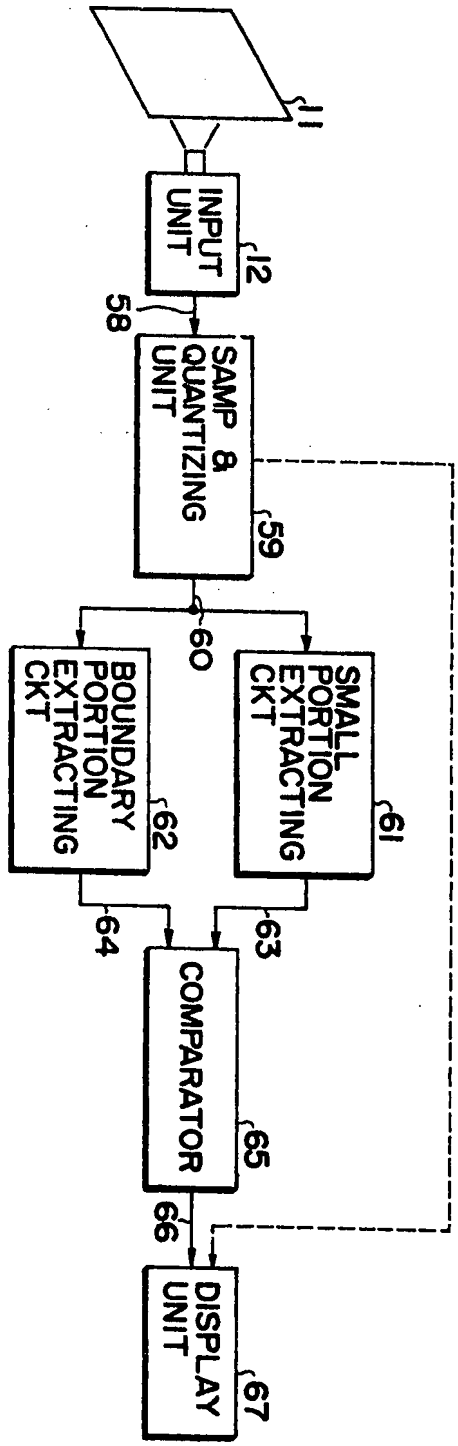
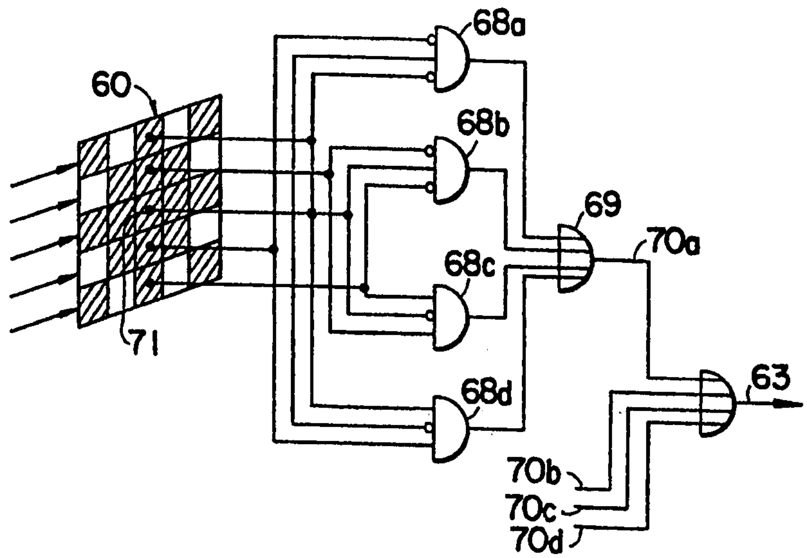

11
INPUT UNIT
12
58
SAMP & QUANTIZING UNIT
59
60
SMALL PORTION EXTRACTING CKT
61
BOUNDARY PORTION EXTRACTING CKT
62
63
64
COMPARATOR
65
66
DISPLAY UNIT
67

FIG. 17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60
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70a
68c
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68d
63
70b
70c
70d

FIG. 18

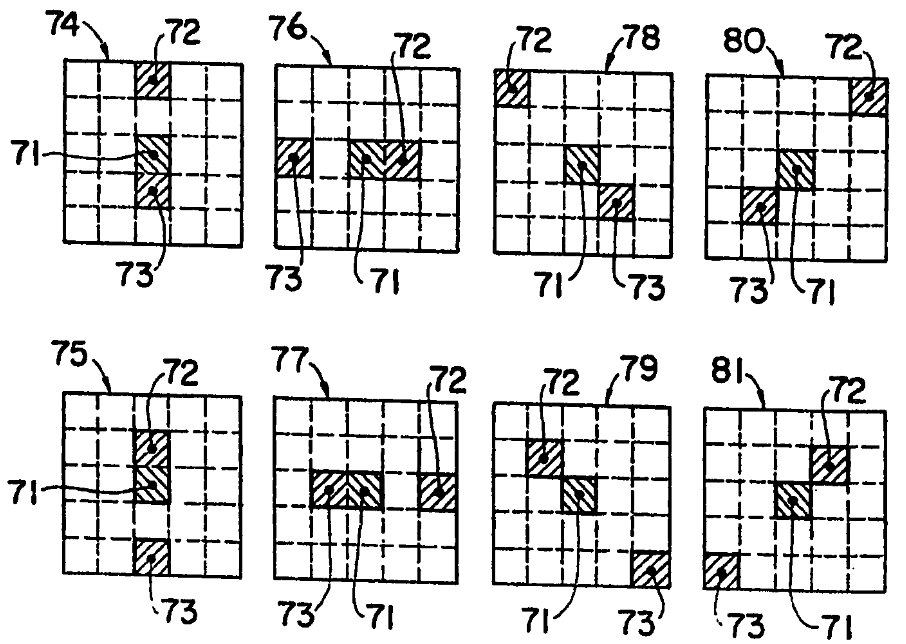
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FIG. 19

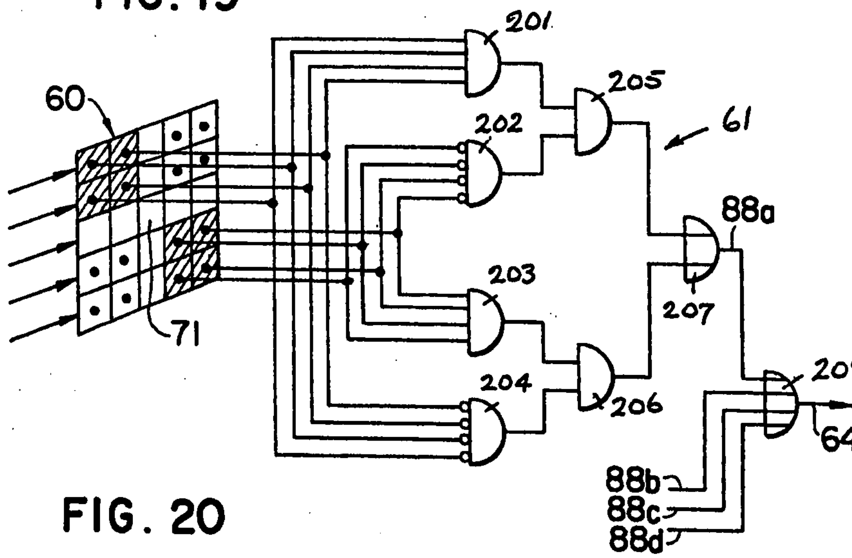


FIG. 20

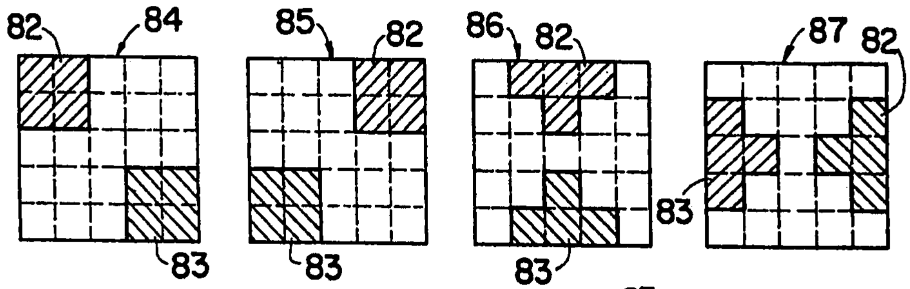
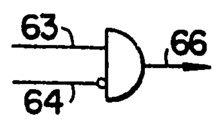


FIG.21



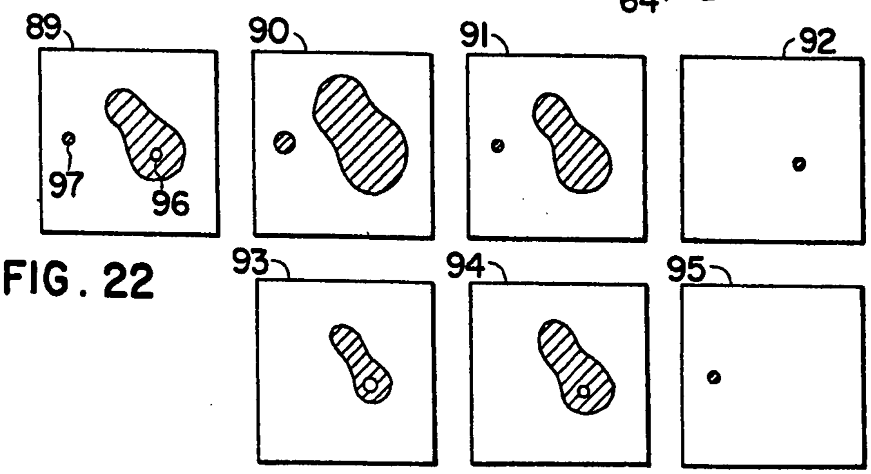


FIG. 22

FIG. 23

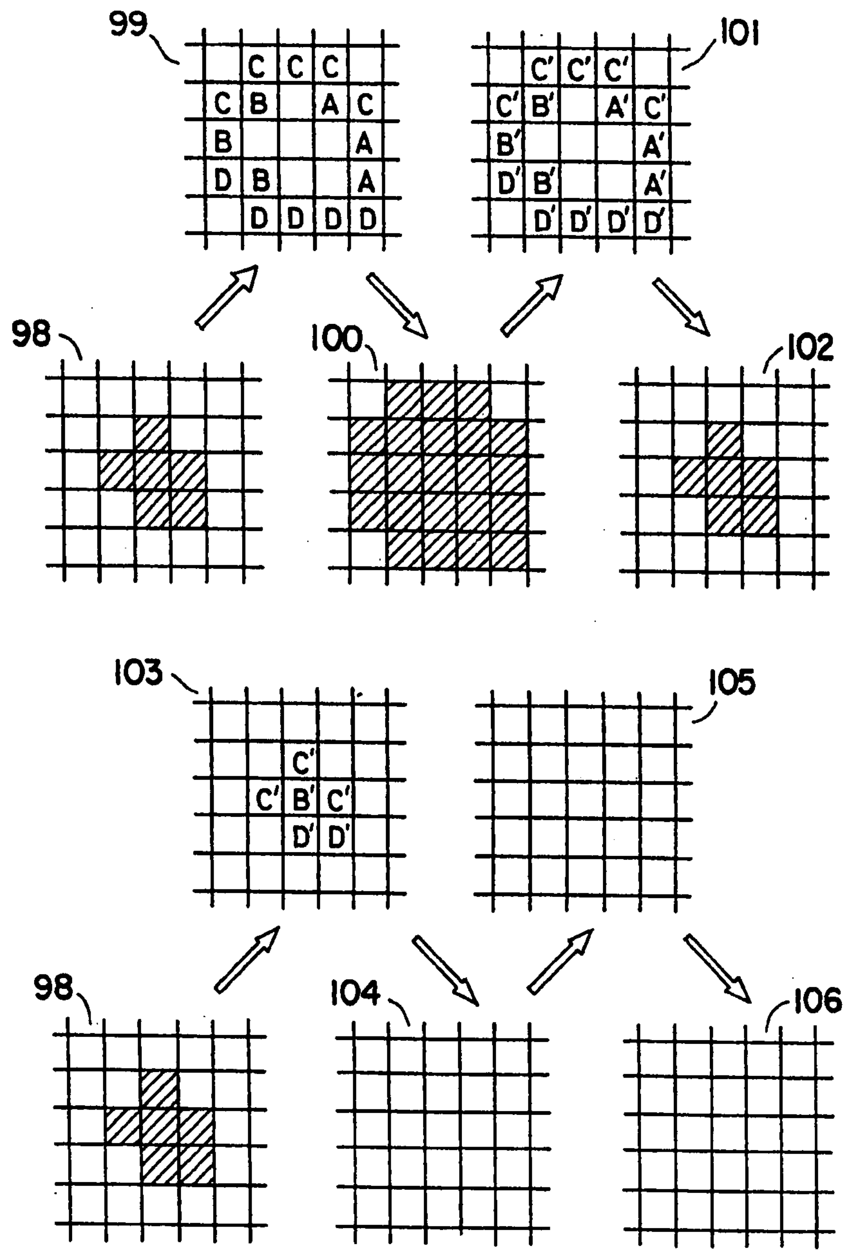

99
C C C
C B A C
B A
D B A
D D D D
101
C' C' C'
C' B' A' C'
B' A'
D' B' A'
D' D' D' D'
98
100
102
103
C'
C' B' C'
D' D'
105
98
104
106

FIG. 24

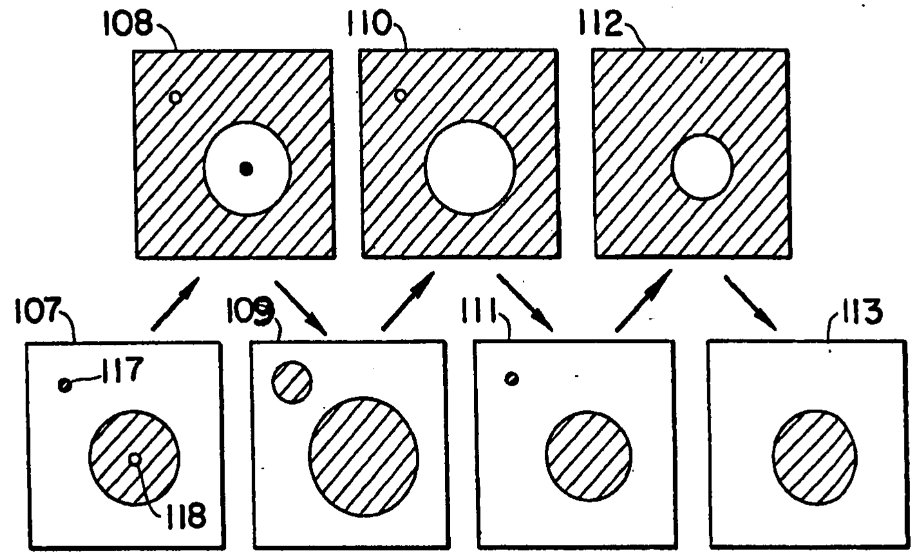


FIG. 25

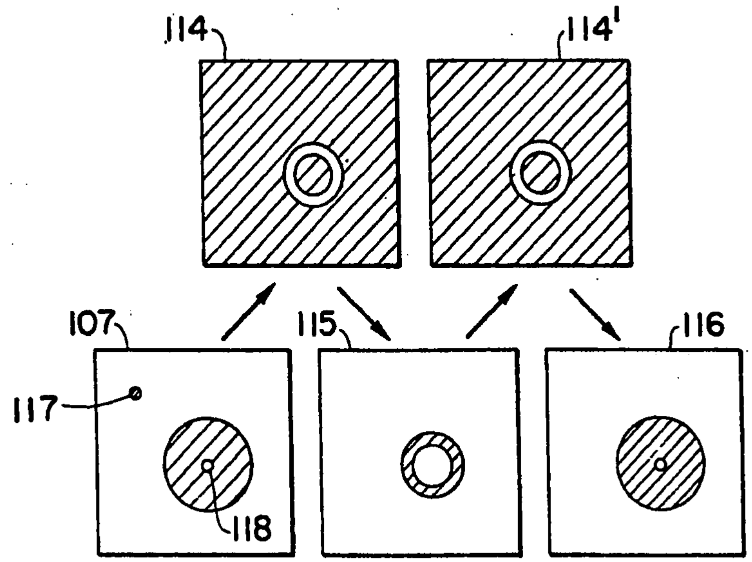


FIG. 26

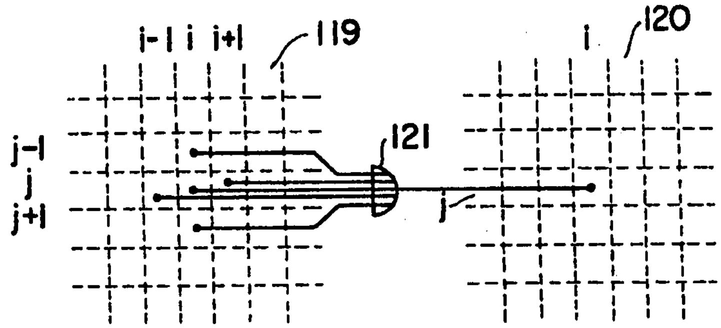


FIG. 27

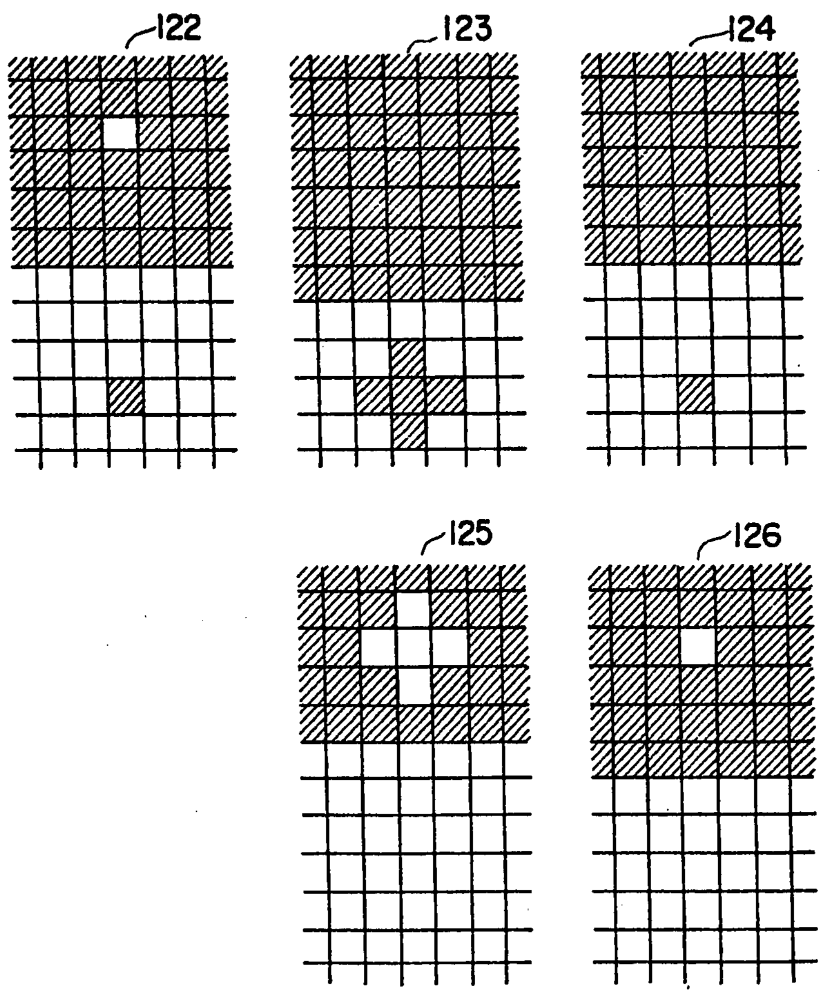


FIG. 28

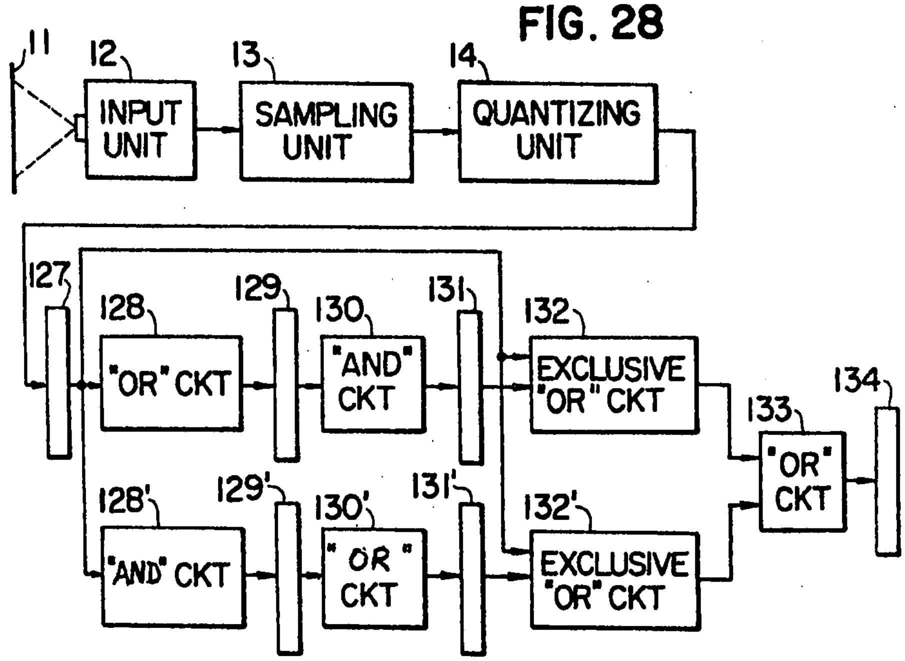


FIG. 29A

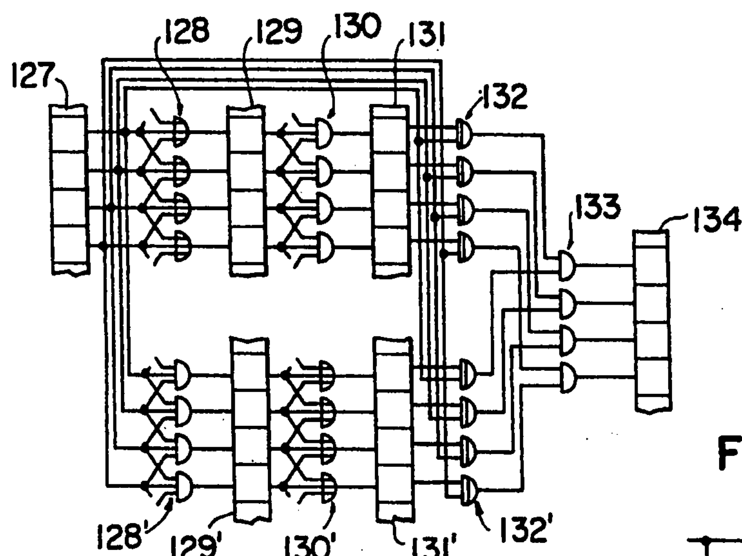


FIG. 29B

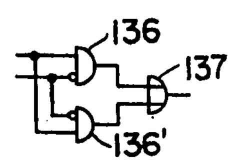


FIG. 30

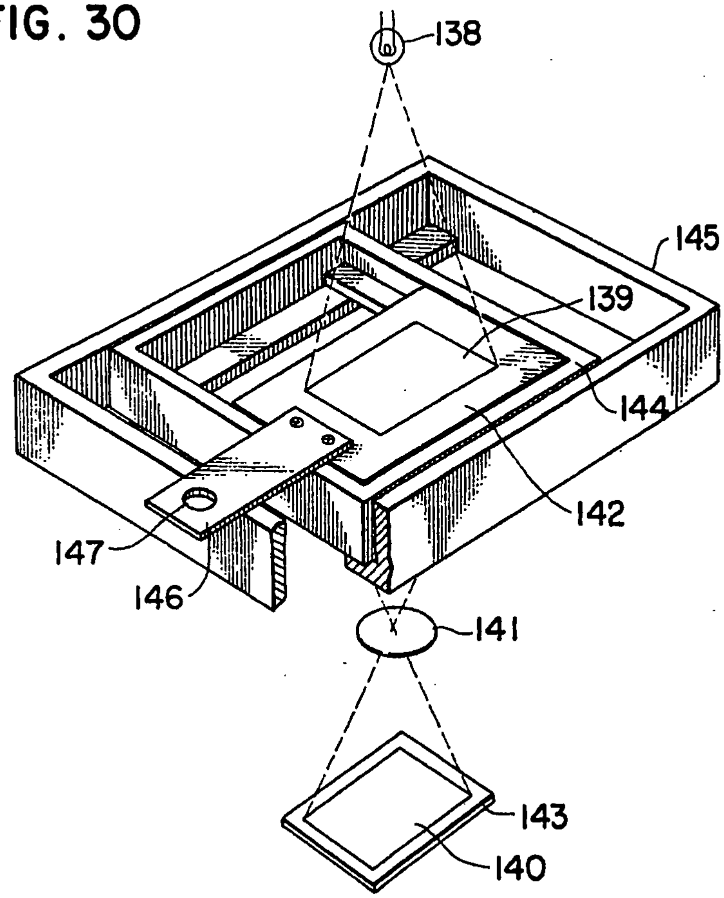
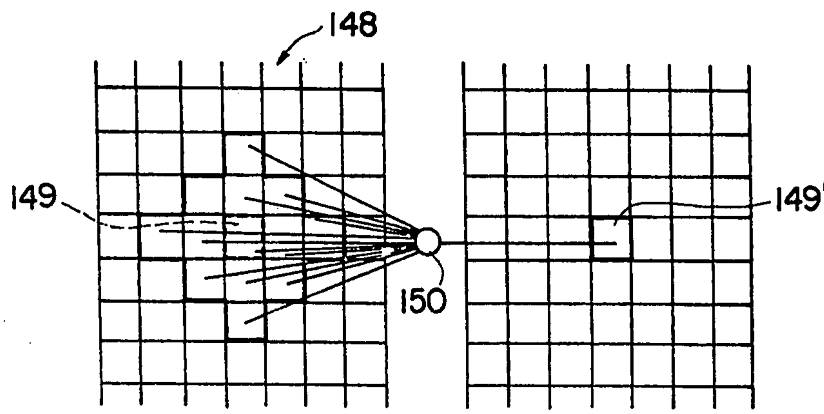


FIG. 31



1 417 721 COMPLETE SPECIFICATION
16 SHEETS *This drawing is a reproduction of the Original on a reduced scale.*
SHEET 13

FIG. 32A

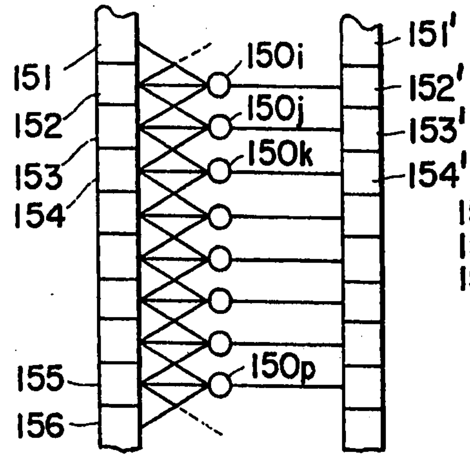


FIG. 32B

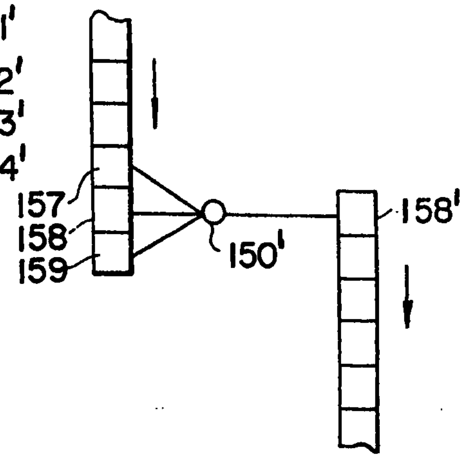


FIG. 33

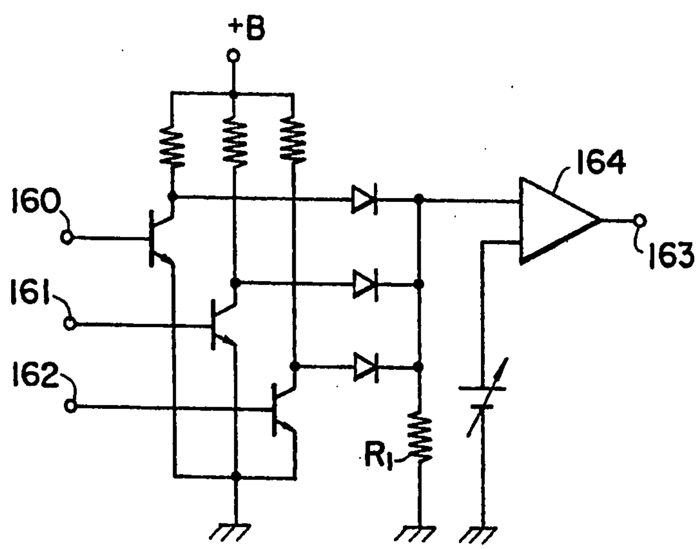


FIG. 34A

0	0	0	1	0	0	0	1	1	1	0	1	1	1	1

FIG. 34B

0	0	1	0	0	0	1	1	1	0	1	1	1	1	1

FIG. 34C

0	0	0	0	1	0	0	0	1	1	1	0	1	1	1

FIG. 34D

0	0	1	1	1	0	1	2	3	2	2	2	3	3	3

FIG. 34E

0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

FIG. 34F

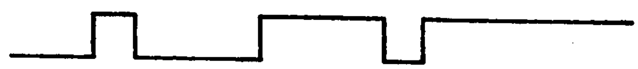

FIG. 34G


FIG. 34H

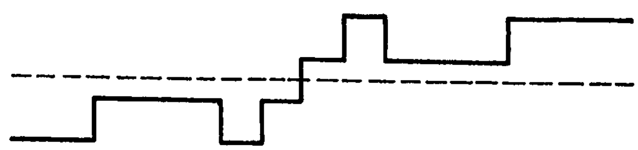

FIG. 34I


FIG. 34J

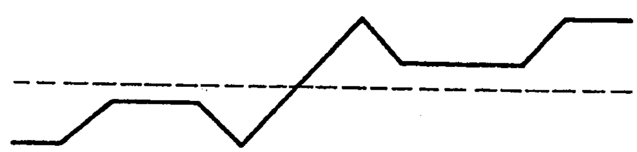

FIG. 34K


FIG. 35

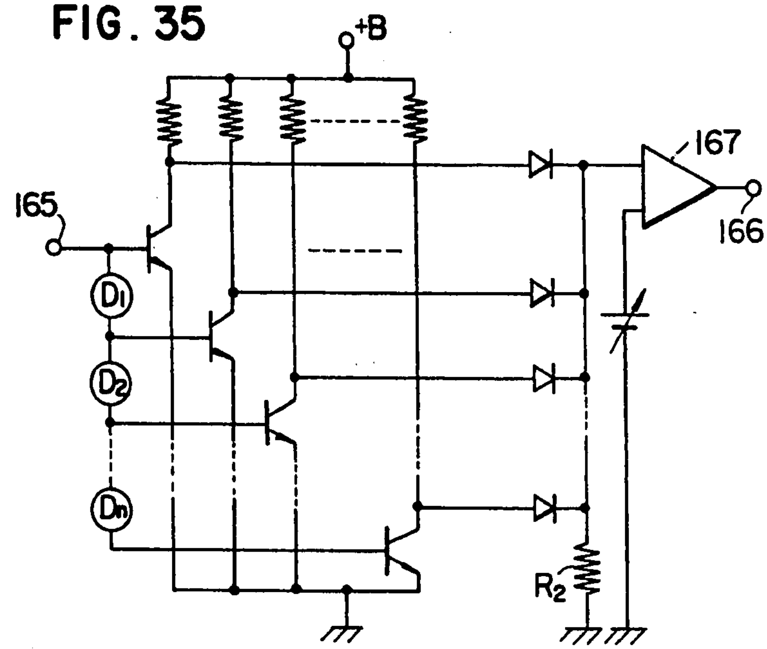


FIG. 36

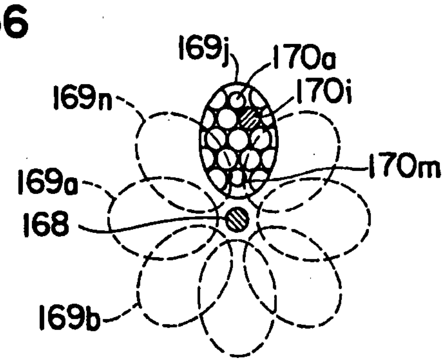


FIG. 37

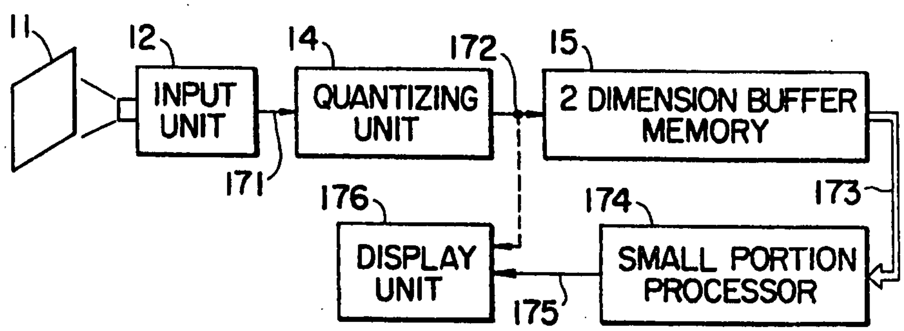


FIG. 38

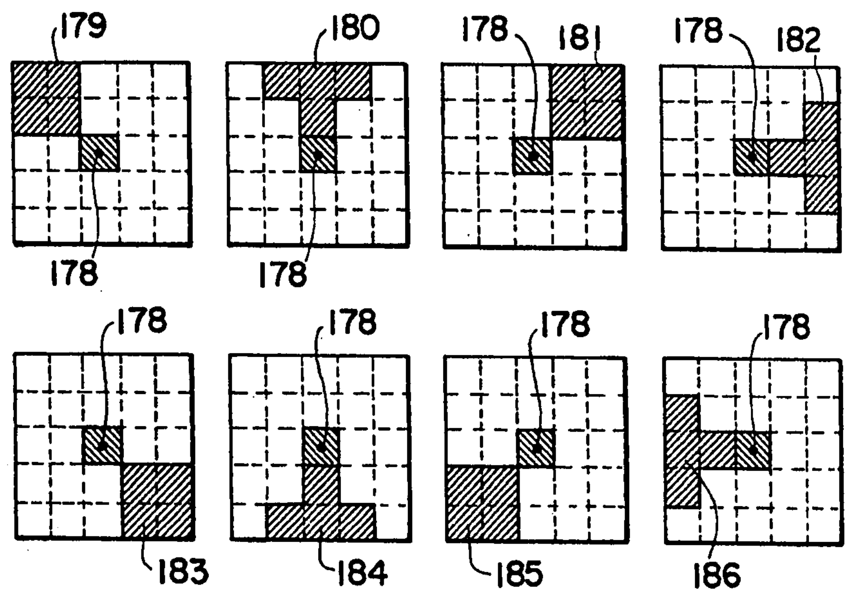

179
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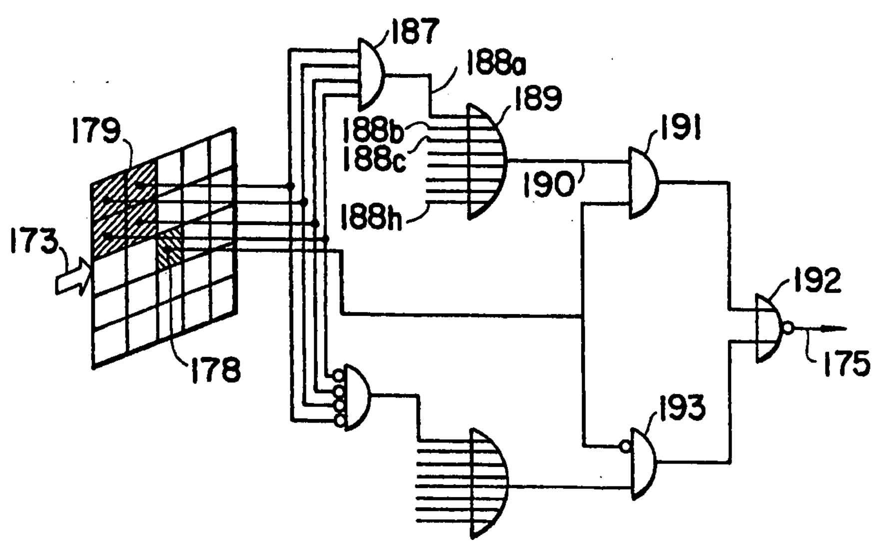
FIG. 39


187
188a
189
188b
188c
188h
190
191
179
173
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